Curriculum
2021

B. Tech.
Electronics and Communication Engineering

(Duration of Study : 4 years)

GMRIT
Training Tomorrow's Engineers Today

Department of Electronics and Communication Engineering
GMR Institute of Technology
Rajam, Andhra Pradesh
(An Autonomous Institute Affiliated to JNTU-GV, Vizinagram, AP)
NBA Accredited and NAAC Accredited

The Vision of GMRIT

- To be among the most preferred institutions for engineering and technological education in the country
- An institution that will bring out the best from its students, faculty and staff – to learn, to achieve, to compete and to grow – among the very best
- An institution where ethics, excellence and excitement will be the work religion, while research, innovation and impact, the work culture

The Mission of GMRIT

- To turnout disciplined and competent engineers with sound work and life ethics
- To implement outcome based education in an IT-enabled environment
- To encourage all-round rigor and instill a spirit of enquiry and critical thinking among students, faculty and staff
- To develop teaching, research and consulting environment in collaboration with industry and other institutions

Department Vision

To be a nationally preferred department of learning for students and teachers alike, with dual commitment to research and serving students in an atmosphere of innovation and critical thinking.

Department Mission

1. To provide high-quality education in Engineering to prepare the graduates for a rewarding career in Electronics and Communication Engineering and related industries, in tune with evolving needs of the industry.

2. To prepare the students to become thinking professionals and good citizens who would apply their knowledge critically and innovatively to solve professional and social problems.

Program Educational Objectives

PEO 1: Embrace technical and professional skills with the spirit of learning, critical thinking while acquiring the fundamentals in science and technology.

PEO 2: Contemplate real life problems, design and develop novel products that are technically viable, economically feasible and socially acceptable.

PEO 3: Encompass ethical values, exhibit soft skills in management & teamwork acquiring leadership qualities.

Program Outcomes

Engineering graduate will be able to

PO 1: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.(Engineering knowledge)

PO 2: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.(Problem analysis)

PO 3: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations. (Design/development of solutions)

PO 4: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.(Conduct investigations of complex problems)

PO 5: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.(Modern tool usage)

PO 6: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.(The engineer and society)

PO 7: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.(Environment and sustainability)

PO 8: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.(Ethics)

PO 9: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.(Individual and team work)

PO 10: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.(Communication)

PO 11: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.(Project management and finance)

PO 12: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.(Life-long learning)

PSO 1: Apply the knowledge of technological evolutions, model / characterize devices and design the integrated circuits to build analog and digital systems. (Program Specific)

PSO 2: Understand and apply the fundamentals of communication and signal processing to develop systems wrapped with industry standard protocols and standards. (Program Specific)

Department of Electronics and Communication Engineering

Minimum Credits to be earned: 160 (for Regular Students)
127 (for Lateral Entry Students)

No	Course Code	Course	POs	Contact Hours			
				L	T	P	C
First Semester							
1	21HSX01	Communicative English	10, 12	2	-	-	2
2	21MAX01	Engineering Mathematics I	1	3	-	-	3
3	21PYX01 21CYX01	Engineering Physics / Engineering Chemistry	1 / 1	3/3	-	-	3/3
4	21BEX01 21BEX06	Basics of Engineering / IT Workshop	1,12/1,12	3/ -	-	-/ 3	3/1.5
5	21BEX02	Problem Solving and Programming Skills	1, 12	3	-	-	3
6	21BEX03	Problem Solving and Programming Skills Lab	4	-	-	3	1.5
7	21BEX04/ 21BEX05	Engineering Drawing / Engineering Workshop	1,5,10/1,9,10	-	-	3/3	1.5/1.5
8	21PYX02/ 21CYX02	Engineering Physics Lab /Engineering Chemistry Lab	4/4	-	-	3/3	1.5
9	21HSX02/-	Communicative English Lab/-	10,12	-	-	3/-	1.5/-
			Total	**14/11**	**0**	**12/12**	**20/17**
Second Semester							
1		Language Elective	10,12	2	-	-	2
2	21MAX02	Engineering Mathematics II	1	3	-	-	3
3	21CYX01/ 21PYX01	Engineering Chemistry /Engineering Physics	1/1	3/3	-	-	3/3
4	21BEX01/ 21BEX06	Basics of Engineering/ IT Workshop	1,12/1,12	-/3	-	3/-	1.5/3
5	21BEX07	Python Programming	1,12	3	-	-	3
6	21BEX08	Python Programming Lab	4	-	-	3	1.5
7	21BEX05/ 21BEX04	Engineering Workshop / Engineering Drawing	1,9,10/1,5,10	-	-	3/3	1.5/1.5
8	21CYX02/ 21PYX02	Engineering Chemistry Lab/Engineering Physics Lab	4/4	-	-	3/3	1.5/1.5
9	-/21HSX02	-/Communicative English Lab	-/10,12	-	-	-/3	-/1.5
			Total	**11/14**	**0**	**12/12**	**17/20**
Third Semester							
1	21MA301	Complex Variables	1, PSO2	3	-	-	3
2	21EC301	Electronic Devices and Circuits	1,2,PSO1	3	-	-	3
3	21EC302	Linear Circuit Analysis	1,2,4,5, PSO1	3	-	2	4
4	21EC303	Logic Circuit Design	1,2, PSO1	3	-	-	3
5	21EC304	Random Variables and Stochastic Processes	1,2, PSO2	3	-	-	3
6	21EC305	Signals & Systems	1,2,4,5, PSO2	3	-	2	4
7	21EC306	Electronic Devices and Circuits Lab	1, 2, 4, PSO1	-	-	3	1.5
8	21EC307	Logic Circuit Design Lab	1, 2, 4, 5, PSO1	-	-	3	1.5
9	21ESX01	Employability Skills I	1,2,5,8,10,12	-	-	2	-
10	21HSX11	CC & EC Activities I	6,7,9,10	-	-	1	-

			Total	**18**	**0**	**13**	**23**
Fourth Semester							
1	21CSE01	Object Oriented Programming	1,2, 5	3	-	-	3
2	21EC401	Analog and Digital Communications	1,2, PSO2	3	-	-	3
3	21EC402	Analog Electronic Circuits	1, 2, 4,5, PSO1	3	-	2	4
4	21EC403	Electromagnetic Fields and Waves	1,2, PSO2	3	-	-	3
5	21EC404	Linear Control Systems	1, 2, PSO1, PSO2	3	-	-	3
6	21CSE02	Object Oriented Programming Lab	1,2,4,5	-	-	3	1.5
7	21EC405	Analog and Digital Communications Lab	1, 2, 4,5, PSO2	-	-	3	1.5
8	21ESX01	Employability Skills I	1,2,5,8,10,12	-	-	2	2
9	21HSX11	CC & EC Activities I	6,7,9,10	-	-	1	1
			Total	**15**	**0**	**11**	**22**
Fifth Semester							
1	21EC501	Linear and Digital IC Applications	1,2, PSO1	3	-	-	3
2	21EC502	Microprocessors and Microcontrollers	1, 2, 3, 4, 5, PSO1	3	-	2	4
3	21EC503	VLSI Design	1, 2,3, 4, 5, PSO1	3	-	2	4
4	21EC504	Antennas and Microwave Engineering	1,2, PSO2	3	-	-	3
5		Elective I (Professional Elective)		3	-	-	3
6		Elective II (Open Elective I)		3	-	-	3
7	21EC505	Linear IC Applications Lab	1,2,3, 4, PSO1	-	-	3	1.5
8	21TPX01	Term Paper	1,4,10,12	-	-	3	1.5
9	21ESX02	Employability Skills II	1,2,5,8,10,12	-	-	2	-
10	21HSX12	CC & EC Activities II	6,7,9,10	-	-	1	-
11	21SIX01	Summer Internship I	1,2,8,10,12	-	-	-	1
			Total	**18**	**0**	**13**	**24**
Sixth Semester							
1	21HSX10	Engineering Economics and Project Management	10,11,12	3	-	-	3
2	21EC601	Cellular and Mobile Communications	1,2, PSO2	3	-	-	3
3	21EC602	Digital Signal Processing	1,2, PSO2	3	-	-	3
4		Elective III (Professional Elective)		3	-	2	4
5		Elective IV (Open Elective II)		3	-	-	3
6	21EC603	Digital Signal Processing Lab	1,2,4,5, PSO2	-	-	3	1.5
7	21MPX01	Mini Project	ALL	-	-	3	1.5
8	21ESX02	Employability Skills II	1,2,5,8,10,12	-	-	2	2
9	21HSX12	CC & EC Activities II	6,7,9,10	-	-	1	1
10	21ATX01	Environmental Studies	1,6,7,12	-	-	-	-
11	21ATX02	Human Values and Professional Ethics	----------	-	-	-	-
12	21ATX----	Audit Course	----------	-	-	-	-
			Total	**15**	**0**	**11**	**22**
Seventh Semester							
1	21PWX01	Project Work	ALL	-	-	16	8
2		Elective V (Professional Elective)		3	-	-	3
3		Elective VI (Professional Elective)		3	-	-	3
4		Elective VII (Open Elective III)		3	-	-	3

5	21SIX02	Summer Internship II	1,2,8,10,12	-	-	-	1
			Total	**9**	**0**	**16**	**18**
Eighth Semester							
1	21FIX01	Full Semester Internship (FSI)	1,2,5,8,9,10, PSO1, PSO2	-	-	**-**	8
2		Elective VIII (Professional Elective)		-	-	**-**	3
3		Elective IX (Open Elective IV)		-	-	**-**	3
			Total	**0**	**0**	**-**	**14**

List of Electives

Language Electives							
No.	**Course Code**	**Course**	**POs**	**Contact Hours**			
				L	**T**	**P**	**C**
1	21HSX03	Advanced Communicative English	10,12	2	-	-	2
2	21HSX04	Communicative German		2	-	-	2
3	21HSX05	Communicative French		2	-	-	2
4	21HSX06	Communicative Japanese		2	-	-	2
5	21HSX07	Communicative Spanish		2	-	-	2
6	21HSX08	Communicative Korean		2	-	-	2
7	21HSX09	Communicative Hindi		2	-	-	2
Elective I							
Career Path I, II, III and Other Core Electives							
1	21ECC11	RTL Coding Techniques (Chip Design Career Path)	1, 2, 3, PSO1	3	-	-	3
2	21ECC21	Data Acquisition System (Embedded System Design Career Path)	1, 2, PSO1	3	-	-	3
3	21ECC31	Information Theory and Coding Techniques (Communication and Signal Processing)	1, 2, PSO2	3	-	-	3
4	21IT304	Database Management Systems	1, 2, 3	3	-	-	3
5	21CS303	Data Structures	1, 2	3	-	-	3
6	21CS403	Computer Organization and Architecture	1,2	3	-	-	3
		MOOCs		-	-	-	3
Elective II:Open Elective I							
1	21CE001	Disaster Management	2,7	3	-	-	3
2	21EE001	Electrical Installation, Safety and Auditing	2,3,6,8	3	-	-	3
3	21ME001	Fundamentals of Optimization Techniques	1,2,3,5	3	-	-	3
4	21EC001	Sensors for Engineering Applications	1	3	-	-	3
5	21CS001	Fundamentals of Artificial Intillegence	1,2,3	3	-	-	3
6	21CH001	Energy Conversion and Storage Devices	1,3,6,7	3	-	-	3
7	21IT001	Fundamentals of Multimedia	3,5,7	3	-	-	3
8	21BS001	Nano Materials and Technology	1,12	3	-	-	3
Elective III							
Career Path I, II, III and Other Core Electives							
1	21ECC12	ASIC Verification using system Verilog (Chip Design Career Path)	1, 2, 3,4,5, PSO1	3	-	2	4
2	21ECC22	Embedded System Design and IoT (Embedded System Design Career Path)	1, 2, 3, 4, 5, PSO1	3	-	2	4
3	21ECC32	Image processing (Communication and Signal Processing)	1, 2,4,5, PSO2	3	-	2	4
4	21EC004	Virtual Instrumentation	1, 2, 4, 5, PSO2	3	-	2	4
5	21EC005	Cryptography and Network Security	1, 3, 4, 5, PSO1	3	-	2	4
6	21CS503	Computer Networks	1,2,4,5,PSO1,PSO2	3	-	2	4
Elective IV : Open Eletive II							
1	21CE002	Air Pollution and Environmental Impact Assessment	6,7,12	3	-	-	3
2	21EE002	Renewable Energy Sources	2,7	3	-	-	3
3	21ME002	Principles of Entrepreneurship	1,5,8,11	3	-	-	3
4	21EC002	Electronics for Agriculture	1,2	3	-	-	3

5	21CS002	Fundamentals of Machine Learning	2,5	3	-	-	3
6	21CH002	Industrial Safety and Hazard Management	1,2,3,6,8	3	-	-	3
7	21IT002	Fundamentals of Cloud Computing	2,6,7,8,12	3	-	-	3
8	21BS002	Advanced Numerical Technquies	1,2	3	-	-	3
9	21BS003	Functional Materials and Applications	1,4	3	-	-	3
Elective V							
Career Path I, II, III and Other Core Electives							
1	21ECC13	Analog and mixed signal VLSI design (Chip Design Career Path)	1, 2, 3, PSO1	3	-	-	3
2	21ECC23	Real Time Operating Systems (Embedded System Design Career Path)	1,2, PSO1	3	-	-	3
3	21ECC33	Multimedia communications (Communication and Signal Processing)	1, 2, PSO2	3	-	-	3
4	21EC007	Wireless Sensor Networks	1, 2, PSO1, PSO2	3	-	-	3
5	21IT403	Operating Systems	1, 12	3	-	-	3
6	21CS603	Software Engineering	4, 5, 8, 11, PSO1	3	-	-	3
		MOOCs		-	-	-	3
Elective VI							
1	21EC008	Design for testability	1, 2, 3, PSO1	3	-	-	3
2	21EC009	Biomedical Signal Processing	1, 2, PSO2	3	-	-	3
3	21EC010	UHF and EHF communication systems	1, 2, PSO2	3	-	-	3
4	21EC010	Neural Networks and Deep Learning	1, 2, PSO1, PSO2	3	-	-	3
		MOOCs		-	-	-	3
Elective VII:Open Elective III							
1	21CE003	Solid Waste Management	2,3,12	3	-	-	3
2	21EE003	Fundamentals of Electrical Vehicle Technology	2,3,12	3	-	-	3
3	21ME003	Industrial Engineering and Management	1,10,11,12	3	-	-	3
4	21EC003	Interfacing and Programming with Arduino	1,2	3	-	-	3
5	21CS003	Data Science for Engineering Applications	2,3,4	3	-	-	3
6	21CH003	Industrial Ecology for Sustainable Development	2,6,7	3	-	-	3
7	21IT003	Fundamentals of Mobile Computing	1,2,7,12	3	-	-	3
8	21BS004	Advanced Materials of Renewable Energy	1,7	3	-	-	3
9	21BS005	Applied Linear Algebra for Engineers	1,12	3	-	-	3
Elective VIII (Professional Elective)							
1	21EC012	Real-Time Systems Design and Analysis	1, 2, PSO1	-	-	-	3
2	21EC013	Image Processing for Engineering Applications	1, 2, PSO2	-	-	-	3
3	21EC014	Computer Architecture	1, 2, PSO1	-	-	-	3
Elective IX:Open Elective IV							
1	21CE019	Green Buildings	2,3,4,5,7	-	-	-	3
2	21EE017	Sustainable Energy	1,2,12	-	-	-	3
3	21ME018	Total Quality Management	1,10,11,12	-	-	-	3
4	21EC011	Communication Technologies	1,2	-	-	-	3
5	21CS020	Applications of Artificial Intelligence	2,3,6,7	-	-	-	3
6	21CH016	Green Technologies	1,6,7	-	-	-	3
7	21IT015	Human Computer Interaction	1,7	-	-	-	3
8	21BS006	Handling of Industrial waste and waste water	1,7	-	-	-	3

Audit Course							
1	21AT001	Communication Etiquette in Workplaces	-	-	-	-	-
2	21AT002	Contemporary India: Economy, Policy and Society	-	-	-	-	-
3	21AT003	Design The Thinking	-	-	-	-	-
4	21AT004	Ethics and Integrity	-	-	-	-	-
5	21AT005	Indian Heritage and Culture	-	-	-	-	-
6	21AT006	Intellectual Property Rights and Patents	-	-	-	-	-
7	21AT007	Introduction to Journalism	-	-	-	-	-
8	21AT008	Mass Media Communication	-	-	-	-	-
9	21AT009	Science, Technology and Development	-	-	-	-	-
10	21AT010	Social Responsibility	-	-	-	-	-
11	21AT011	The Art of Photography and Film Making	-	-	-	-	-
12	21AT012	Gender Equality for Sustanibity	-	-	-	-	-
13	21AT013	Women in Leadership	-	-	-	-	-
14	21AT014	Introduction to Research Methodology	-	-	-	-	-
15	21AT015	Climate Change and Circular Economy	-	-	-	-	-
B. Tech. (Honors)							
Domain I VLSI Circuit Design and Verification							
01	21ECH11	SoC Design	1,2,PSO1	4	-	-	4
02	21ECH12	CMOS Logic Circuit Design	1, 2, 3, PSO1	4	-	-	4
03	21ECH13	Low Power VLSI Design	1, 2, 3, PSO1	4	-	-	4
04	21ECH14	VLSI Fabrication Technology	1,2,3, PSO1	4	-	-	4
Domain II Robotics and Automation							
01	21ECH21	Advanced Controllers	1, 2, 3, PSO1	4	-	-	4
02	21ECH22	Robots and Control	1, 2, 3, PSO1	4	-	-	4
03	21ECH23	Industrial Automation	1, 2, PSO1, PSO2	4	-	-	4
04	21ECH24	Distributed Embedded systems	1, 2, 3, PSO1	4	-	-	4
Domain III Cognitive Radio Networks							
01	21ECH31	Optical Communications	1, 2, PSO2	4	-	-	4
02	21ECH32	MIMO Wireless Communications	1,2,3, PSO2	4	-	-	4
03	21ECH33	Software Defined Radio	1, 2,PSO2	4	-	-	4
04	21ECH34	Wireless and Mobile Networks	1, 2, PSO1	4	-	-	4
Domain IV Multimedia Signal Processing							
01	21ECH41	Optimization Techniques	1, 2,PSO1, PSO2	4	-	-	4
02	21ECH42	Audio Signal Processing	1,2,3,PSO2	4	-	-	4
03	21ECH43	Statistical Signal Processing	1,2,3,PSO2	4	-	-	4
04	21ECH44	Computer Vision	1,2,PSO2	4	-	-	4
B. Tech. (Minors)							
Energy Science & Technology							
01	21CHM11	Foundation of Energy Science and Technology	1,2,3,5,7,12	4	-	-	4
02	21CHM12	Energy Generation from Waste	1,2,3,4,5	4	-	-	4
03	21CHM13	Energy Storage Systems	1,2,3,6,7	4	-	-	4
04	21CHM14	Hydrogen Energy and Fuel Cells	1,2,3,7	4	-	-	4
Nano Science & Technology							
01	21CHM21	Introduction and Characterization of Nano Materials	1,2,3,7	4	-	-	4
02	21CHM22	Carbon Nanostructures and Applications	1,3,4,5	4	-	-	4
03	21CHM23	Energy, Environment & Biomedical Nanotechnology	1,2,3,7	4	-	-	4
04	21CHM24	Industrial Applications of Nano Technology	2,3,5,7	4	-	-	4
Environmental Engineering							

01	21CEM11	Watershed Management	6,7	4	-	-	4
02	21CEM12	Industrial Pollution Control and Engineering	3,6,7,12	4	-	-	4
03	21CEM13	Solid and Hazardous Waste Management	1,3,6,7	4	-	-	4
04	21CEM14	Ecology and Environmental Assessment	1,3,6,7	4	-	-	4
Artificial Intelligence & Machine Learning							
01	21CSM11	Fundamentals of AI & Machine Learning	1,12	4	-	-	4
02	21CSM12	Feature Engineering for Machine Learning	1,2,3	4	-	-	4
03	21CSM13	Exploratory Data Analytics	1,4	4	-	-	4
04	21CSM14	Deep Learning	1,2,4	4	-	-	4
Cyber Security							
01	21CSM21	Fundamentals of Security	1,2	4	-	-	4
02	21CSM22	Management of Information Security	3,6,7	4	-	-	4
03	21CSM23	Cyber Security	1,3,4	4	-	-	4
04	21CSM24	Cloud Security	2,3	4	-	-	4
Data Science & Analytics							
01	21CSM31	Data Cleaning	2,3,4	4	-	-	4
02	21CSM32	Data Engineering	1,2,3,4	4	-	-	4
03	21CSM33	Text Analytics	1,2,4	4	-	-	4
04	21CSM34	Social Network and Semantic Analysis	2,4	4	-	-	4
Computer Systems Programming							
01	21CSM41	Programming Fundamentals	1,2,3	4	-	-	4
02	21CSM42	Data Structures & Algorithms	1,2,3,4	4	-	-	4
03	21CSM43	Fundamentals of Databases	1,4	4	-	-	4
04	21CSM44	Fundamentals of Computer Networks & Operating Systems	1,2,3	4	-	-	4
Digital IC Design							
01	21ECM11	Fundamentals of VLSI Design	1,2,3	4	-	-	4
02	21ECM12	Digital Design using HDL	1,2,3	4	-	-	4
03	21ECM13	FPGA Technology	1,2	4	-	-	4
04	21ECM14	Analog and Mixed Signal Design	1,2	4	-	-	4
Industrial Automation							
01	21ECM21	Microcontrollers and Interfacing	1,2,3	4	-	-	4
02	21ECM22	Sensors and Data Acquisition System	1,2	4	-	-	4
03	21ECM23	Fundamentals of Labview	1,2	4	-	-	4
04	21ECM24	Medical Robotics	1,2,3	4	-	-	4
Communications and Networking							
01	21ECM31	Principles of Communications	1,2	4	-	-	4
02	21ECM32	Coding Theory and Practice	1,2	4	-	-	4
03	21ECM33	Ad-hoc and Wireless Sensor Networks	1,2,3	4	-	-	4
04	21ECM34	Fundamentals of Multimedia Networking	1,2,3	4	-	-	4
Avionics							
01	21ECM41	Principles of Aerodynamics	1,2	4	-	-	4
02	21ECM42	Aircraft Electrical Systems	1,2	4	-	-	4
03	21ECM43	Aircraft Instrument Systems	1,2	4	-	-	4
04	21ECM44	Aircraft Communication and Navigational Systems	1,2	4	-	-	4
Geographic Information System							
01	21ECM51	Sensors and Sensing Technology	1,2	4	-	-	4
02	21ECM52	Geographic Information Systems	1,2	4	-	-	4
03	21ECM53	Digital Image Processing	1,2	4	-	-	4
04	21ECM54	Lidar Systems	1,2	4	-	-	4
Electric Vehicles and Technology							
01	21EEM11	Introduction to Electric Vehicles Technologies	1,2,3	4	-	-	4
02	21EEM12	Electrical Drives and Controllers for	1,2,3	4	-	-	4

		Electric Vehicles					
03	21EEM13	Charging Technology in Electric Vehicles	1,2,3	4	-	-	4
04	21EEM14	Computer Vision in Electric Vehicles	1,2,3	4	-	-	4
Smart City Management							
01	21EEM21	Fundamentals of Smart City	2,3	4	-	-	4
02	21EEM22	Smart City Infrastructure	1,2,3,5,6,7,11	4	-	-	4
03	21EEM23	Computational Methods for Smart City Management	3,5	4	-	-	4
04	21EEM24	Communication Technologies and Mobility for Smart City	2,3	4	-	-	4
Industrial Applications and Control							
01	21EEM31	Modeling and Simulations of Industrial Applications	1,2,3	4	-	-	4
02	21EEM32	Industrial Sensors and Actuators	1,2,3	4	-	-	4
03	21EEM33	Programmable Logic Controllers	1,2,3	4	-	-	4
04	21EEM34	Control Design for Industrial Applications	1,2,3	4	-	-	4
Cloud Application Development							
01	21ITM11	Introduction to Cloud Computing	6,7,12	4	-	-	4
02	21ITM12	Introduction to Web Development with HTML, CSS, JavaScript	1,2,3,9,12	4	-	-	4
03	21ITM13	Developing Cloud Native Applications	5,8,10	4	-	-	4
04	21ITM14	Developing Cloud Apps with Node.js and React	5,8,10	4	-	-	4
Robotics and Automation							
01	21MEM11	Introduction to Robotics	1,2,3	4	-	-	4
02	21MEM12	Drives and Sensors	1,2,3,4	4	-	-	4
03	21MEM13	Control Systems for Robotics	1,2,3,4	4	-	-	4
04	21MEM14	Machine Learning for Robotics	2,5	4	-	-	4
Industrial Systems Engineering							
01	21MEM21	Industrial Management	1,10,11,12	4	-	-	4
02	21MEM22	Fundamentals of Operations Research	1,2,3,5	4	-	-	4
03	21MEM23	Enterprise Resource Planning	1,2,3,5,11,12	4	-	-	4
04	21MEM24	Production Planning and Control	1,2,3,5,11,12	4	-	-	4

21MA301 Complex Variables

(Programme: ECE)

3 0 0 3

Course Outcomes

1. Understand the knowledge of Bessel's and Legendre's functions for solving engineering problems
2. Infer the calculus of complex valued functions with Cauchy-Riemann equations
3. Use Cauchy's theorem and Integral formulae to compute complex integrals
4. Outline the singularities of complex variable function Taylor's, Laurent's series
5. Select Residue theorem to determine various types of definite integrals
6. Compute calculus of complex functions and conformal mappings

COs – POs Mapping

COs	PO_1	PSO_2
1	2	2
2	2	2
3	3	3
4	3	3
5	3	3
6	3	3

[1] 3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Special Functions

Bessel functions – Generating function, Jacobi series, Recurrence relations, Orthogonality, related problems Legendre's functions- Generating function, Rodrigue's formula, Recurrence relations, Orthogonality, related problems

Chebyshev's polynomials of first kind and second kind

12 Hours

Unit II

Functions of a complex variable and complex integration

Functions of a complex variable – Continuity, Differentiability, Analyticity, Properties, Cauchy-Riemann equations in Cartesian and polar coordinates (without proof), Harmonic and conjugate harmonic functions, Milne – Thomson method

Complex integration- Line integral, evaluation along a path and by indefinite integration, Cauchy's integral theorem, Cauchy's integral formula, Generalized integral formula (without proofs)

Elementary functions: General and principal values of elementary functions

12 Hours

Unit III

Complex power series and contour integration

Complex power series- Radius of convergence, Taylor's series, Maclaurin's series and Laurent series (without proofs)

Singular point –Types of singularities, Residue – Evaluation of residues, Residue theorem (without proof) Evaluation of integrals of the type

(a) Improper real integrals $\int_{-\infty}^{\infty} f(x)dx$ (b) $\int_{c}^{c+2\pi} f(\cos\theta, \sin\theta)d\theta$ (c) $\int_{-\infty}^{\infty} e^{imx} f(x)dx$

The Laplace inversion integral-Stability Criteria and evaluation of integrals by indentation

12 Hours

Unit IV
Calculus of complex functions and conformal mappings

Argument principle, Rouche's theorem - determination of number of zeros of complex polynomials, Maximum Modulus principle, Fundamental theorem of Algebra, Liouville's Theorem (Theorems without proof)

Conformal mapping -Translation, rotation, inversion, Transformation by e^z, z^2, z^n (n positive integer), sin z, cos z, z + a/z
Bilinear transformation – fixed point, properties, invariance of circles and cross ratio, determination of bilinear transformation

The Schwartz-Christoffel Transformation

12Hours
Total: 48 Hours

Textbook (s)

1. R.K.Jain and S. R. K Iyengar, Advanced Engineering Mathematics, Narosa Publishing House, 4th Edition, New Delhi, 2014
2. B.S.Grewal, Higher Engineering Mathematics, Khanna Publishers,42nd Edition, New Delhi, 2012
3. B. V. Ramana , Engineering Mathematics, Tata McGraw Hill, New Delhi, 4th Edition,2009

Reference (s)

1. Kreyszig, Irvin, Advanced Engineering Mathematics, Wiley India Pvt. Ltd, 9th Edition, 2012
2. T.K.V. Iyengar et. al, Engineering Mathematics, Volume-III, S. Chand Co., 2ndEdition, New Delhi, 2007
3. Ray Wylie and C.Louis Barrett, Advanced Engineering Mathematics, Tata McGraw-Hill PublishingCom. Ltd, 6th Edition, 2003

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open book exam (%)
Remember	10	10	-
Understand	30	30	-
Apply	60	60	70
Analyze	-	-	30
Evaluate	-	-	-
Create	-	-	-
Total (%)	100	100	100

Remember

1. State the steps involved in solving difference equation using Z-transforms.
2. Define analytic function and write C-R equations in polar form.

Understand

1. Prove that $\int_C \frac{dz}{z-a} = 2\pi i$ where C is $|z-a| = r$
2. Interpret the transformation $w = \frac{1}{z}$ to find the image of $|z - 2i| = 2$ in complex plane.

Apply

1. Use Z-transforms to solve difference equation $u_{n+2} - u_n = 2^n$ with $u_0 = 0$ and $u_1 = 1$.
2. Implement residue theorem to evaluate the definite integral $\int f(z)dz$ over the circle $|z| = 2.5$

and $f(z) = \frac{z^2}{(z-1)^2(z+2)}$.

Analyze

1. Classify singularities of a complex valued function and also illustrate the examples for different types of singularities.
2. Justify that the function $f(z) = \sqrt{|xy|}$ is not analytic at the origin, although C-R equations are satisfied at that point.
3. Let $\phi(x, y)$ be an electrical potential in the region that satisfies the boundary values

$$\phi(x,y) = \begin{cases} 100 \quad for \quad C_1 = \left\{ z = e^{i\theta} : 0 < \theta < \frac{\pi}{2} \right\} \\ 0 \quad for \quad C_2 = \left\{ z = e^{i\theta} : \frac{\pi}{2} < \theta < 2\pi \right\} \end{cases} \ldots\ldots(1)$$

and $w = f(z) = \frac{(1-i)(z-i)}{(z-1)}$ is a conformal mapping which maps the unit disc onto the upper half plane.

Here $z = x + iy$ is a point in xy - plane and $w = u + iv$ is a point in uv - plane.

[Open Book Examination Question]

a) Compute the transformed boundary conditions.
b) Determine the electrical potential in the unit disc satisfying the boundary conditions.
c) Estimate the electrical potential in the region bounded by triangle whose vertices are (0,0), (1,0) and (0,1) satisfying the given boundary conditions using suitable conformal mapping.

4. If $F(z) = -ikz(k > 0)$ describes a uniform flow upward, which can be interpreted as a uniform flow between two parallel lines,
   a. What happens to the flow if you replace z by $ze^{-i\pi/4}$ in $F(z)$?
   b. Obtain a flow around a corner using suitable conformal mapping.

[Open Book Examination Question]

21EC301 Electronic Devices and Circuits

3 0 0 3

Course Outcomes

1. Explain operation of semiconductor devices, characteristics and their applications
2. Illustrate the characteristics of BJT and JFET
3. Construct different biasing circuits for BJT
4. Illustrate h-parameter representation and Hybrid-model of transistor
5. Analyse low frequency and high frequency single stage amplifiers
6. Construct multi stage amplifiers

COs – POs Mapping

COs	PO_1	PO_2	PSO_1
1	2		2
2	2		2
3	3	2	3
4	2		2
5	3	2	3
6	3	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Semiconductors–Diodes

PN junction diode - Forward bias and Reverse bias, Volt-ampere characteristics of p-n diode, Transition and Diffusion capacitances, Zener diode characteristics, Tunnel Diode characteristics - Energy band diagrams, UJT characteristics and SCR characteristics. Rectifiers - Half wave rectifier, Full wave center Tapped , Bridge rectifier, Capacitor filter, Regulator using Zener diode.

Special diodes and it's applications

12 Hours

Unit II

BJT & FET

Bipolar Junction transistors **-** Transistor current components, Transistor as an amplifier, Relation between Alpha and Beta, Input and Output characteristics of Common Base and Common Emitter configurations , BJT biasing - Criteria for fixing operating point, Fixed bias, Collector to base bias, Self-bias, Stabilization techniques, Compensation techniques- Compensation against variation in V*BE* and I*co*, Thermal run away, Thermal stability, Characteristics of JFET.

MOSFET characteristics- Enhancement mode and depletion mode

13 Hours

Unit III

Low Frequency Amplifiers

h-parameter representation of a transistor, Analysis of single stage transistor amplifier using h-parameters - Voltage gain, Current gain, Input impedance and Output impedance of CE, CB, and CC amplifiers using exact and approximate analysis. Miller's and Dual of Miller's theorem.

Analysis of single stage FET amplifiers - voltage gain, input impedance and output impedance of CS, CG, and CD amplifiers.

Buffer amplifier, MOSFET Amplifier

12 Hours

Unit IV

High Frequency and Multi Stage Amplifiers

Hybrid -CE transistor Model, Determination of Hybrid -Conductances, CE Short Circuit Current gain, Parameters of f_β and f*T* , Frequency response of RC coupled CE amplifiers. n–Stage Cascaded Amplifier, Darlington pair, Cascode amplifier, CE-CC Amplifiers.

Transformer coupled amplifier, CE current gain with load

11 Hours

Total: 48 Hours

Textbook (s)

1. J.Millman, C.C.Halkias and Chetan D Parikh, Integrated Electronics, 2nd Edition, Tata McGraw Hill, 2017
2. Robert L. Boylestad and Louis Nashelsky, Electronic Devices and Circuits Theory, Pearson/Prentice Hall, 11th Edition, 2015

Reference (s)

1. A.Salivahanan, N.Suresh Kumar, A.Vallavaraj, Electronic Devices and Circuits, Tata McGraw-Hill Publish-ing Company Limited, 2nd Edition, 2008
2. Visvesvara Rao, K. Bhaskara Rama Murty, K. Raja Rajeswari, P.Chalam Raju Pantulu, Electronic Devices and Circuits, Pearson Education, 2nd Edition, 2007
3. Millman and Grabel, Microelectronics, Tata McGraw Hill, 7thEdition, 2001
4. S.G.Burns and P.R.Bond, Principles of Electronic Circuits, Galgotia Publications, 2nd Edition, 1998

Sample Question (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	20	20	--
Understand	55	40	--
Apply	25	40	60
Analyse	--	--	40
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. List any two advantages of JFET over BJT.
2. Define Rectifiers. List any two types of Rectifiers.
3. Define stability factor, S.
4. Reproduce the symbol of n type JFET.
5. Reproduce the symbol of p type JFET.
6. Arrange emitter, base and collector in increasing order of doping concentration.

Understand

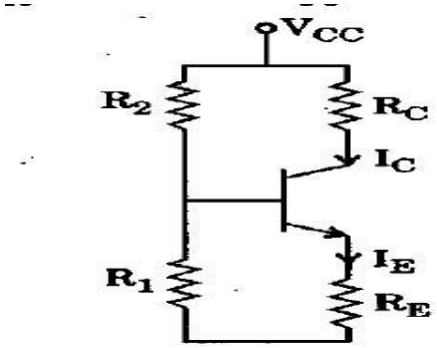
1. Explain the consequences due to applied reverse voltage at Collector junction in CB configuration.
2. Represent the structure of JFET and explain the operation of n channel JFET.
3. Illustrate the current components of BJT.
4. Interpret FET as a Voltage Controlled Device.
5. Compare compensation techniques for the variations in ICO due to temperature.
6. Explain about thermal runaway.
7. Explain the Breakdown Mechanism in Semiconductor Diodes.
8. Explain the working principle of Tunnel diode with its V-I characteristics.

Apply

1. Find the value of IC and IE of a transistor at room temperature for Ico=5μA, IB=100μA and β= 100, If the temperature is raised by 100°C.
2. A full wave rectifier is designed with a 50μF capacitor in parallel with a 500Ω resistor. The transformer secondary voltage to centre-tap is 40V rms and 50Hz. The diode and transformer resistances may be ne-glected. Compute the followings:
   (i) Ripple factor of the rectifier-filter output
   (ii) % of load regulation

(iii) Repeat (i) and (ii) if 100μF capacitor in parallel with a 500Ω resistor.

3. Design a Self-biasing circuit as shown in figure such that IC= 5mA, VCE=8V, VE=6V, S=10, β=200 and VCC=20V.



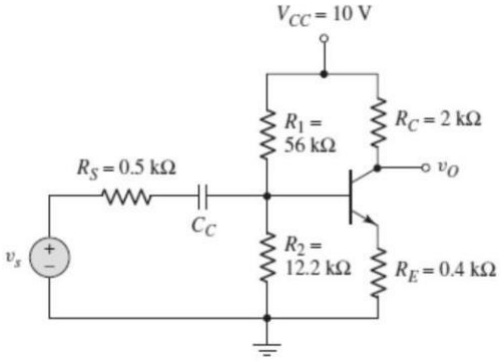
4. A circuit designer team-A has to design a biasing circuit using BC182 transistor. The purpose of biasing circuit is to produce faithful amplification to the input signal if the circuit operates in temperature range of 25°C to 75°C. The circuit designer team-B has provided the information to Team-B that if the operating point of the biasing circuit varies between (11.3mA, 5.67V) to (17mA, 2.48V) then also faithful amplifica-tion can be achieved. Design the biasing circuit.

5. A designer has to design a base resistor bias circuit for a CE amplifier such that operating point is VCE=8Vand IC = 2 mA. He is supplied with a fixed 15V d.c. supply and a transistor with β = 100. Take base-emitter voltage VBE = 0.6V and he has the liberty to use silicon or germanium transistor. Calculate also the value of load resistance that would be employed.

[Open Book Examination Question]

Analyse

1. Justify the small-signal voltage gain and input resistance of a common-emitter circuit with an emitter resistor.
   For the circuit in below figure, the transistor parameters are: β = 100, VBE(on) = 0.7 V.



2. A high frequency amplifier uses a transistor which is driven from a source with Rs=0. Calculate value of fH, if RL =0 and RL=1kΩ. Assume typical values of hybrid-π parameters.

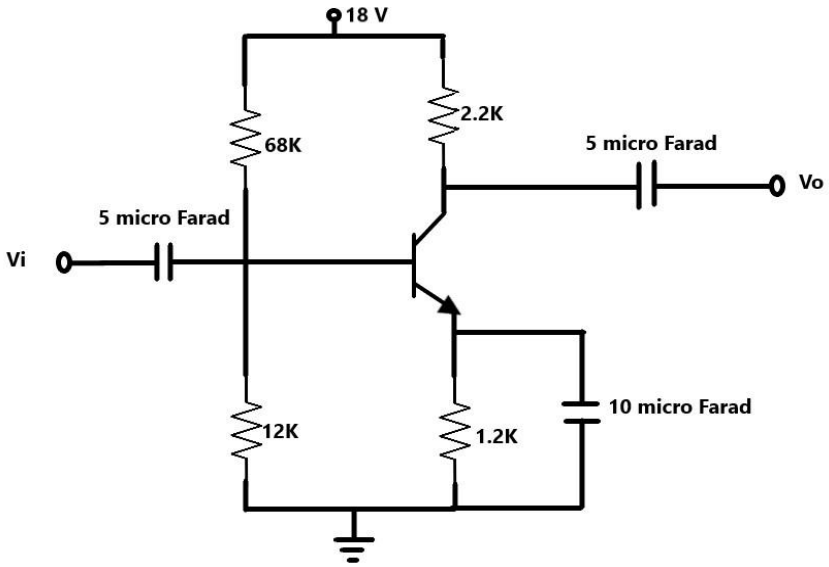
3. A circuit shown is to be a part of larger circuit which is expected to be operated at 25°C and 1000 Hz frequency. As a design engineer you are supposed determine the following parameters using the exact hybrid equivalent model and to prepare a detailed comparative analysis report of the results obtained using the approximate analysis.

(a) Input impedance and overall input impedance.

(b) Current gain and overall current gain.

(c) Voltage gain and overall voltage gain.

(d) Output impedance and overall output impedance.



[Open Book Examination Question]

21EC302 Linear Circuit Analysis

3 0 2 4

Course Outcomes

1. Interpret the characteristics of RL, RC, RLC series and parallel circuits in both time and frequency domain
2. Compute the power and power factor of RL, RC, RLC series and parallel circuits
3. Design resonant circuits for a given frequency
4. Demonstrate the theorems to simplify complex networks
5. Assess the transient behaviour of RLC circuits
6. Compute the parameters of two port networks

COs – POs Mapping

COs	PO_1	PO_2	PO_4	PO_5	PSO_1
1	2		1	2	2
2	3	2	1	2	3
3	3	2	2	2	3
4	3	2	2	2	3
5	3	2	2	2	3
6	3	2	2	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Sinusoidal Steady State Analysis

Concept of Phasor and J notation, Impedance and Admittance – Time domain and frequency domain response of R, L, C series, parallel and series- parallel circuits to sinusoidal excitation. Computation of active, reactive, complex power and power factor, Series and parallel resonance of RLC circuits –Selectivity, bandwidth and quality factor-implications with voltage and current excitation.

Incandecent Lamp, Tube light

Practical Components

1. Verification of series RLC circuits.
2. Verification of parallel RLC circuits.
3. Verification of Source power factor for the random RLC Circuit.
4. Verification of series Resonance circuits.
5. Verification of Parallel Resonance circuits.

13+10 Hours

Unit II

Network Theorems

Source transformation, Superposition, Thevinin's, Norton's, Maximum power transfer, Reciprocity, Tellegen's, Millman's and Compensation theorems for DC and AC excitations.

Substitution theorem Miller's Theorem

Practical Components

1. Analysis of linear circuits using superposition Theorem.
2. Analysis of linear circuits using Thevenins Theorem.
3. Analysis of linear circuits using Nortons theorem.
4. Alysis of linear circuits using Compensation Theorem.
5. Verification of Maximum power transfer theorem

11+10 Hours

Unit III

Transient Analysis

D.C Transients: Transient response of R-L, R-C, R-L-C circuits for d.c excitation – initial conditions –solution using differential equations and Laplace transform approaches.

A.C Transients: Transient response of R-L, R-C, R-L-C circuits for sinusoidal excitation – initial conditions – Solution using Laplace transform approaches.

Transient behavior of RLC circuits for Impulse excitation,Transient behavior of RLC circuits for Ramp excitation

Practical Components

1. Time constant of a RL (series & parallel) circuits.
2. Time constant of a RC (series & parallel) circuits.

15+4 Hours

Unit IV

Network Parameters

Two port networks, Impedance parameters, Admittance parameters, Transmission parameters, hybrid parameters – Interrelationship between parameters – Concept of transformed network – two port network parameters using transformed variables – Interconnection of two port networks.
BJT equivalent circuit, Characteristic impedance of Two port networks

Practical Components

1. Measurement of Impedance parameters of linear circuits.
2. Measurement of Admittance parameters of linear circuits.
3. Measurement of Hybrid parameters of linear circuits
4. Measurement of ABCD parameters of linear circuits

9+8 Hours
Total: 48+32 Hours

Textbook (s)

1. M.E Van Valkenburg, Network Analysis, Prentice Hall of India, 3rd Edition, 2015
2. W.H.Hayt, J.E.Kimmerly, and S.M.Durb, Engineering circuit analysis, McGraw Hill Education private limited, 8th Edition, 2013

Reference (s)

1. Gopal G. Bhise, Prem R. Chadha,Durgesh C. Kulshreshtha, Engineering Network Analysis and Filter Desgin, Umesh Publications, 2009
2. Charles K Alexander, Mathew N.O Sadiku, Fundamentals of Electric circuits, Tata McGraw Hill, 5th Edition
3. Sudhakar A, Shyammohan S Palli, Circuits and Networks: Analysis and Synthesis, McGraw Hill, 5th Edition

Sample Question (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Lab Examination (%)
Remember	25	25	--
Understand	35	35	--
Apply	40	40	100
Analyze	--	--	--
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. Define power factor, active power, reactive power and apparent power.
2. Define Maximum Power transfer theorem.
3. Define Nortons theorem.
4. Draw the Two Port network using Y parameters
5. A series-connected circuit has R = 4Ω & and L = 25 mH. Calculate the value of 'C' that will produce a quality factor of 50.
6. Define resonant frequency.
7. Draw the circuit of a low-pass T-section filter.
8. Define Thevinens theorem.

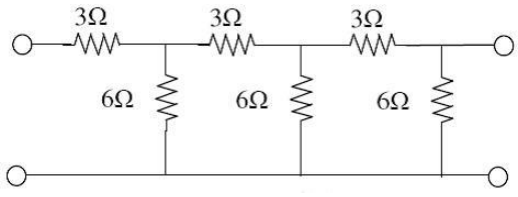
Understand

1. Draw a power triangle for L-C-R parallel circuit.
2. Explain the principle of superposition.
3. Explain the uses of various types of filters.
4. Explain sinusoidal steady state response of the series RL circuit and derive expressions for the voltage across R, voltage across L and the current flowing through the circuit.
5. The voltage across a 1-μF capacitor is 10V for t < 0. At t = 0, a 1-MΩ resistor is connected across the capacitor terminals. Find the time constant τ, and the expression for v(t).
6. The current in a series circuit of R = 5Ω and L= 30mH lags the applied voltage by 800.Determine the source frequency and the impedance Z.
7. What do you mean by cut off frequency?
8. Explain the operation of L.C. Filter.

Apply

1. Design a T and ∏ section constant-K high pass filter having cut-off frequency of 10 kHz and nominal impedance is 500Ω. Also find i) its characteristic impedance and phase constant at 25kHz.
2. Determine the Y- parameters of the network shown in fig. and also find Z- parameters

i.



3. Express z-parameters in terms of h-parameters and ABCD-parameters.
4. Find the current response when a series RL circuit is connected to a sudden ac voltage Vs = V0cosωt.
5. A series RC circuit with R = 5kΩ and C = 20 mF has a constant-voltage source of 100V applied at t = 0; there is no initial charge on the capacitor. Obtain i, and q, for t > 0.
6. Obtain an expression for resonance frequency of parallel circuit considering internal resistances of inductance and capacitance.

21EC303 Logic Circuit Design

3 0 0 3

Course Outcomes

1. Illustrate binary codes (weighted and non-weighted) and convert a number from one number system to an-other
2. Identify a suitable tool (Boolean theorems, K-maps, Tabular etc.) to minimize Boolean expressions
3. Implement combinational circuits using AOI and Universal logic gates
4. Design combinational logic circuits using PLDs
5. Analyse sequential logic circuits
6. Differentiate Mealy and Moore machines

COs – POs Mapping

COs	PO_1	PO_2	PSO_1
1	2		2
2	2		2
3	3	2	3
4	3	2	3
5	3	2	3
6	3	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Number Systems and Boolean Algebra

Review of number systems, Conversion of numbers from one radix to another radix, Complements, Signed Binary Numbers, Floting point representation, Weighted and Non weighted codes, Basic Gates - NOT, AND, OR, Boolean theorems, Dual of logical expressions, Universal Gates - EX-OR and EX-NoR, SOP, POS, Minimization of logic functions using Boolean theorems, Two level realization of logic functions using universal Gates, Error detection and Error correction codes, Parity checking - even parity, odd parity, Hamming code.

Burglar Alarm, Door Bell, Enable gate and Inhibit gate

12 Hours

Unit II

Boolean Function minimization and Combinational Logic Circuits

Minimization of Boolean functions up to four variables using Karnaugh Map - POS and SOP, with Don't Care Conditions, Minimization of Boolean functions using Tabular method, Combinational logic circuits - Half adder, Full adder, Half subtractor, Full subtractor, Comparator, Ripple carry adder, Carry look ahead adder, Encoder, Priority encoder, Decoder, Multiplexer, De-Multiplexer, Code converters, Realization of switching functions using combinational logic circuits.

GATES using MUX and Demultiplexers

12 Hours

Unit III

PLDs and Flip Flops

Programmable logic devices – PROM, PAL, PLA , Realization of Switching functions using PROM, PAL and PLA. Sequential logic circuits – RS latch using NAND and NOR Gates, Flip Flops – RS, JK ,T and D ,Truth tables and Excitation Tables, Conversion of Flip Flops, Asynchronous Inputs .

Realisation of Flip Flops using MUX, Glue logic

12 Hours

Unit IV

Sequential Logic Circuits

Registers - Buffer register, Controlled buffer register, Shift registers, Bi-directional shift register, Universal shift register, Asynchronous & Synchronous counters - Up, Down, Up down, Ring counters,Johnson counters, Mealy and Moore state machines - Conversion, Reduction of state tables and state assignment.

Sequence Generator, Sequence detector

12 Hours

Total: 48 Hours

Textbook (s)

1. A. Anand Kumar, Switching theory and logic design,PHI,3rd Edition 2016
2. Morris Mano, Digital Design,3rd Edition, PHI, 2001

Reference (s)

1. Zvi Kohavi, Switching & Finite Automata theory, 2nd Edition, TMH, 2008
2. R P Jain, Modern Digital Electronics, 3rd Edition, TMH, 2003

Sample Question (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	25	25	--
Understand	50	25	--
Apply	25	50	75
Analyse	--	--	25
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

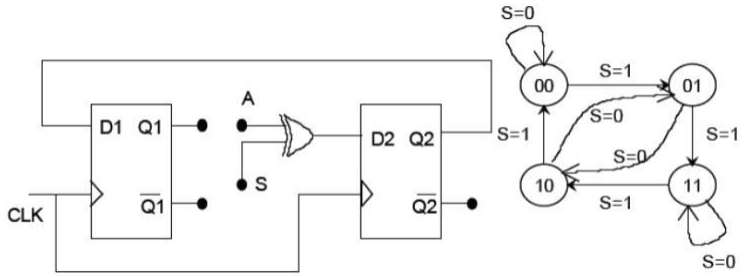
1. Retrive the decimal value of the fractional binary number 0.1011.
2. List any two postulates of Boolean algebra.
3. List the four uses of decoders.
4. Define Flip flop.
5. Define asynchronous sequential circuit.
6. List the difference between Synchronous and asynchronous

Understand

1. Explain how digital circuits are more frequently constructed with NAND or NOR gates than with AND & OR gates.
2. Represent the following Boolean expression to minterms and maxterms A+BC'+ABD'+ABCD.
3. Represent the Boolean function T=F (w, x, y, z)= $\sum$ m (0,1,2,4,5,7,8,9,12,13) by using 8 to 1mux.
4. Illustrate a half adder using NAND – NAND.
5. Represent a JK flip flop using SR flip flop.
6. Explain the operation of T-flip-flop.

Apply

1. Design a 4bit binary adder using Finate state machine.
2. In a certain application, four inputs A, B, C, D (both true and complement forms available) are fed to logic circuit, producing an output F, which operates a relay. The relay turns on when F(ABCD) = 1 for the following states of the inputs (ABCD):'0000', '0010', '0101', '0110', '1101' and '1110'. States '1000' and '1001' do not occur, and for the remaining states, the relay is off. Minimize F with the help of a Karnaugh map and realize it using a minimum number of 3 – input NAND gates.
   [Open Book Examination Question]
3. The digital logic shown in the figure satisfies the given state diagram when Q1 is connected to input A of the XOR gate. Suppose the XOR gate is replaced by an XNOR gate, from the following options predict the option which one preserves the state diagram (A) Input A is connected to compliment of 2 (B) Input A is connected to 2 (C) Input A is connected to compliment of 1 and S is complemented (D) Input A is connected to compliment of Q1.



[Open Book Examination Question]

Analyse

1. Consider Eight people in a row identify number of males among them by using a Full adder.Note: consider Male=1 and female =0.
2. A milk vendor delivers one milk packet every day on some days he may not in a position to deliver the milk packet for various logistic reasons. There are 7 binary variable (D1, D2,…..D7) representing the delivery status every day (Di is 1 if milk is delivered else it is 0).Design a combinational circuit with minimum number of full adders to represent the sum of milk packets delivered in one week. Find the expression to calculate the amount of money to be paid if the cost of the milk per packet is Rs.15.Money is represented by M3 M2 M1 M0 and sum of milk packets is represented by S2 S1 S0).
   [Open Book Examination Question]

3. In a function hall, entry in to it is restricted to one person per minute. If the clock frequency is 1/60Hz, design a digital circuit to identify the number of groups formed entered in the following manner. Note: Male, Female, Male.
   [Open Book Examination Question]

21EC304 Random Variables and Stochastic Processes

3 0 0 3

Course Outcomes

1. Exemplify the probability theory concepts and Bayes theorem.
2. Illustrate the distribution and density functions of random variable.
3. Compute the moments of random variable.
4. Represent the statistical properties of multiple random variables.
5. Compute the joint moments and their functions.
6. Analyse the statistical characteristics of random processes.

COs – POs Mapping

COs	PO_1	PO_2	PSO_2
1	2		2
2	2		2
3	3	2	3
4	2		2
5	3	2	3
6	3	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked.

Unit I

Probability Theory

Set theory, Classical definition of Probability, Probability as a Relative Frequency, Axioms of probability, properties, equality of events, borel fields, Joint Probability, Conditional Probability, Total Probability, Bayes' Theorem, Independent Events, Mutually Exclusive events, combined sample space, permutations, combinations, bernoulli trails. *Outage probability, Entropy*

11 Hours

Unit II

The Random Variable

Definition of a Random Variable, Conditions for a Function to be a Random Variable, Discrete and Continuous random variables, Distribution function, Density functions, Examples of random variables: Binomial, Poisson, Uniform, Gaussian, Exponential, Rayleigh, Conditional Distribution and density function, Expectation, Moments, Functions that give moments: Moment generation function, Characteristic function, Transformation of random variable. *Chebyshev Inequality, Chernoff bound, Schwarz Inequality*

13 Hours

Unit III

Multiple Random Variables

Vector random variables, Joint Distribution Function and properties, Marginal Distribution Functions, Joint density function and properties, Marginal density function, Conditional distribution and density, Statistical independence, Expectation, Joint moments, Joint moment generating function, Joint characteristic function, Jointly Gaussian random variable, Sum of random variables, central limit theorem.
Geometric random variable, Convergence of random variables

12 Hours

Unit IV

Random Processes

Temporal Characteristics: The Random Processes, Classification of Random Processes, Stationarity and Independence: Wide Sense Stationary processes, strict sense stationary processes, Time Averages and Ergodicity, Gaussian random processes. Spectral Characteristics: Power Spectral density and its Properties, Relationship between Power Spectrum and Autocorrelation Function, Cross Power Density Spectrum, Properties, Relationship between Cross Power Spectrum and Cross Correlation Function.
Markov processes, Wiener processes

12 Hours

Total: 48 Hours

Textbook (s)

1. A. Papoulis, S. U. Pillai, Probability, Random Variables and Stochastic Processes, 4th Edition, McGraw-Hill, 2002
2. Peyton Z. Peebles, Probability, Random Variables & Random Signal Principles, TMH, 4th Edition,2001

Reference (s)

1. Y.Mallikarjuna Reddy, Probability theory and Stochastic Processes, 4th Editions, Universities press, 2013
2. Oliver C Ibe, Fundamentals of applied probability and random process, Elsevier, 2005
3. R. D. Yates and D. J. Goodman, Probability and Stochastic Processes, 2nd Edition, Wiley, 2005
4. S. Haykin, Communication Systems, 4th Edition, John Wiley & Sons, 2001

Sample Question (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	20	15	--
Understand	55	60	--
Apply	25	25	70
Analyse	--	--	30
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. Define probability as a relative frequency
2. Define the following terms: i) Independent events ii) Mutually exclusive events
3. State the conditions for random variable
4. List any two types of random processes

Understand

1. Illustrate Bayes theorem using total probability theorem
2. Summarize the properties of density function
3. Classify the moments of random variable
4. Indicate the conditions for the process to be WSS.

Apply

1. Box 1 contains 2000 diodes of which 10% are defective, Box 2 contains 3000 diodes of which 5% are defective. Two diodes are picked from randomly selected box. Find (a) The probability that both diodes are defective. (b) If both diodes are defective, what is the probability that they came from box 1.

2. Compute the Mean and Variance of Uniform density function having $f(x) = \frac{1}{(b-a)} \quad a \le x \le b$
$= 0 \quad else$

3. Find the constant b such that the given function is valid joint density, and obtain their marginal densities.

$$f(x,y) = \begin{cases} b(x+y)^2 & -2 < x < 2, -3 < y < 3 \\ 0 & else \end{cases}$$

4. You have 1000 dollars to deposit in an account with interest rate R, compounded annually. If the sum assured is $Xn=1000(1+R)^n$ in 'n' years. The interest rate R is a random variable that is determined when you put the money in the bank, but it does not change after that. Let assume that R ~Uniform (0.04,0.05).
   i) Compute all possible sample functions for the random process Xn, {n=0,1,2,...}.
   ii) Find the expected value of your account at year three E[X3].
   iii) Find the mean functions for the random processes.
   iv) Compute the correlation functions and covariance functions for the random processes.
   [Open Book Examination Question]

5. As the nature of signal transmission over fading environment under weather conditions. The subscriber not received signal properly because he move from one area to another area. Estimate the expected signal with necessary assumptions.

   a. Hint: Fading – Rayleigh fading, rician fading.
   b. Area: Urban, Rural, Remote Area (FOREST)

   i) Compute the expected value and variance of radio signal using suitable moment function.
   ii) Select the suitable stochastic model of radio propagation under natural disasters with strong signal and Justify.
   [Open Book Examination Question]

Analyse

1. Justify that the average power Pxx of a WSS random process X(t) is defined as the time average of its second moment or autocorrelation function at $\tau = 0$
2. If the autocorrelation of a WSS process is $R_{xx}(\tau) = Ke^{-K|\tau|}$, conclude that its spectral density is given by
   $S(\omega) = 2/[1 +(\omega /K)^2]$
3. Consider a wireless propagation channel, with transmitted signal x(t) and received signal as y(t). Assume the process as stationary and random in nature. Noise is additive at the receiver. Under this scenario, it has mean 2 and the autocorrelation function is $R_{xx}(\tau) = 4 + \exp(-|\tau|/10)$. Outline the mean and variance of received signal $Y = \int_0^1 X(t)dt$

   [Open Book Examination Question]

4. In a radar system, the received signal gets disrupted by the randomness present in the channel, follows the uniform distribution and characteristics exhibits the random properties. Then for a random process
   $X(t) = A\cos\omega_0 t$
   Where ω_o is constant and A is uniformly distributed with mean 5 and variance 2. Outline the average power of X(t).

[Open Book Examination Question]

21EC305 Signals & Systems

3 0 2 4

Course Outcomes

1. Interpret various types of signals and systems and their operations
2. Explain signal approximation using Fourier series
3. Execute Fourier transform and Laplace transform of continuous signals
4. Summarise the characteristics of the LTI system and its properties
5. Compute LTI system response using convolution, correlation
6. Interpret sampling process and it's effects

COs – POs Mapping

COs	PO_1	PO_2	PO_4	PO_5	PSO_2
1	2		2	3	2
2	2		2	3	2
3	3	2	2	3	3
4	2		2	3	2
5	3	2	2	3	3
6	2		2	3	2

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Introduction: Signal Analysis

Classification of Continuous time & Discrete time signals, Concept of impulse function, unit step function, Signum function, Signal operations, Power and Energy of signals, Orthogonal signal space, Signal approximation using orthogonal functions, Mean square error, Orthogonality in complex functions.
EEG, ECG signals

Practical Components

1. Familiarization with SCILAB/MATLAB: Matrix operations, plotting, relational operators, loops and functions
2. Generation of basic signals: Exponential, step, impulse, ramp, sinusoidal signals
3. Operations on signals: time reversal, time shifting
4. Operations on signals: amplitude scaling, time scaling

10+8 Hours

Unit II

Fourier Series and Fourier Transform

Representation of Fourier series for Continuous time periodic signals, Dirichlet's conditions, , properties of Fourier series, Exponential Fourier series, Relationship between Exponential Fourier series and trigonometric Fourier series, Concept of Fourier transform, Fourier transform of arbitrary signal, Fourier transform of standard signals, properties of Fourier transforms, Parseval's theorem, Hilbert Transform, Review of Laplace transforms, Inverse Laplace transform, Concept of region of convergence, Relation between Laplace & Fourier Transform.
Fourier series coefficients of Conjugate symmetry for real signals, Laplace transform of causal periodic signals

Practical Components

1. Find the trigonometric Fourier series coefficients of a rectangular periodic signal and reconstruct the Signal by combining the Fourier series coefficients with appropriate weights
2. Verification of Parseval's theorem
3. Find the Fourier transform of a square pulse. Plot its amplitude and phase spectrum
4. Draw the pole zero plot of given transfer function

14+8 Hours

Unit III

LTI Systems

Linear system, impulse response, Linear time invariant (LTI) system, Transfer function of a LTI system, Filter characteristics of linear systems, Distortionless transmission through a system, Ideal filter characteristics, Causality and Paley-Wiener criterion for physical realization.
Concept of convolution in time domain and frequency domain, Graphical representation of convolution, Cross

correlation and auto correlation of functions, properties of correlation functions, Energy density spectrum, Power density spectrum, Relation between convolution and correlation.
Detection of periodic signals in the presence of Noise by Correlation, Group delay

Practical Components

1. Design the first order low pass passive filter for given specifications and Plot the magnitude and phase response
2. Design the first order high pass passive filter for given specifications and Plot the magnitude and phase response
3. Generate the response of an LTI system for the given input and impulse response
4. Write a program to Check the given system is linear or not

13+8Hours

Unit IV

Sampling Theory

Sampling theorem: Graphical and analytical proof for Band Limited Signals, impulse sampling, Natural and Flat top Sampling, Reconstruction of signal from its samples, Aliasing, Bandpss sampling theorem
Zero-order Hold sampling, Interpolation

Practical Components

1. Find the Nyquist rate for a given signal.
2. Generate a discrete time sequence by sampling a continuous time signal.
3. Reconstruction of a signal from the discrete samples with aliasing effect.
4. Reconstruction of a signal from the discrete samples without aliasing effect.

11+8Hours

Total: 48+32 Hours

Text Book (s)

1. A.V. Oppenheim, A.S. Willsky and S.H. Nawab, Signals and Systems, PHI, 2nd Edition, 2015
2. Won Y Yang, Signals and Systems with MATLAB, Springer publications, 2014
3. B.P. Lathi, Signals, Systems & Communications, BS Publications, 2008

Reference Book(s)

1. Michel J. Robert, Fundamentals of Signals and Systems, MGH International Edition, 2nd Edition 2017
2. Simon Haykin and Van Veen,Wiley, Signals & Systems, PHI, 2nd Edition, 2007
3. C. L. Philips, J.M.Parr and Eve A.Riskin, Signals, Systems and Transforms, Pearson education, 3rd Edi-tion, 2004

Sample Question (S)

Internal Assessment Pattern

Cognitive Level	Int Test 1 (%)	Int Test 2 (%)	Lab Examination (%)
Remember	35	20	--
Understand	40	30	--
Apply	25	50	100
Analyse	--	--	--
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

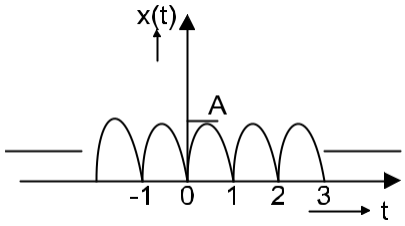
1. Define impulse function.
2. List out any two Dirichlet's conditions.
3. State linearity property.
4. Define Nyquist rate.
5. List out any two types of sampling.
6. Define Laplace Transform
7. Define power and energy signals.

Understand

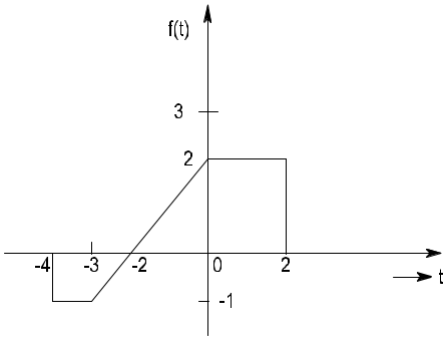
1. Classify two types of continuous time signals
2. Illustrate the relationship between exponential Fourier series and trigonometric Fourier series
3. Compare Autocorrelation and cross correlation function
4. Illustrate the effect of under sampling
5. Explain the properties of Region of convergence
6. Illustrate the orthogonality between two complex functions
7. Explain relation between Laplace and Fourier transform

Apply

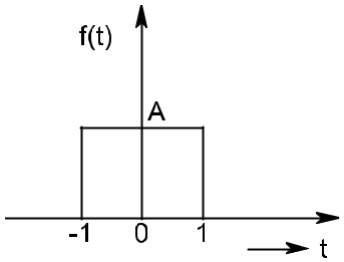
1. Find the trigonometric Fourier series for the given signal.



2. For the given signal x(t), find
   i. x(2t+5) ii. x(-t-2) iii. Even part of x(t)



3. Find the Fourier transform and sketch its frequency spectrum of the following signals
   $x(t) = e^{-4t}\,u(t)$



21EC306 Electronic Devices and Circuits Lab

0 0 3 1.5

Course Outcomes

1. Assess the characteristics of semiconductor devices
2. Find the load and line regulation of rectifiers
3. Implement D.C. Regulated power supply
4. Assess the characteristics of BJT and FET
5. Construct the characteristics of CE and CS amplifiers
6. Assess the frequency response of CE and CS amplifiers

COs – POs Mapping

COs	PO_1	PO_2	PO_4	PSO_1
1	3	2	2	3
2	3	2	2	3
3	3	2	2	3
4	3	2	2	3
5	3	2	2	3
6	3	2	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

List of Experiments
Students will perform minimum twelve Experiments

1. PN Junction diode characteristics
2. Zener diode characteristics
3. Half wave rectifier with and without filter.
4. Full wave center tapped rectifier with and without filter.
5. Bridge type Full wave rectifier
6. Design of Zener regulator.
7. Characteristics of SCR
8. Characteristics of UJT
9. Transistor CE characteristics (Input and Output)
10. Transistor CB characteristics (Input and Output)
11. Design of self-bias circuit
12. JFET characteristics
13. Characteristics of CE Amplifier
14. Characteristics of CS Amplifier
15. Frequency response of CE amplifier
16. Frequency response of CS amplifier

List of Augmented Experiments*

1. Design of Regulated DC Power Supply
2. Applications based on FET
3. Applications based on BJT
4. Applications based on SCR
5. Burglar Alarm

Reading Material (s)

1. N.N.Bhargava, D.C.kulshreshtha S.C.Gupta, Basic electronics and linear circuits Tata MC Graw Hill com-pany Ltd., New Delhi, 2nd Edition, 2003.
2. R.L. Boylestad and Louis Nashelsky, Electronic Devices and Circuits, Pearson/Prentice Hall, 9thEdition, 2006.

* Students shall opt any one of the Augmented experiment in addition to the regular experiments

21EC307 Logic Circuit Design Lab

0 0 3 1.5

Course Outcomes

1. Identify the functionality of Combinational logic ICs
2. Implement the Boolean functions using logic gates and Universal logic gates
3. Design combinational logic circuits using logic gates for a given application
4. Identify the functionality of sequential logic ICs
5. Implement flip-flops using logic gates
6. Design Sequential logic circuits using flip-flops for a given application

COs –POs Mapping

COs	PO_1	PO_2	PO_4	PO_5	PSO_1
1	2		2		2
2	3	2	2		3
3	3	2	2	3	3
4	2		2	3	2
5	3	2	2	3	3
6	3	2	2	3	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

List of experiments

Students will perform minimum twelve Experiments

1. Verification of logic gates and implementation of universal gates by using logic gates.
2. Realization of a Boolean function by using NAND-NAND and NOR-NOR logic.
3. Design a half adder circuit using gates and implement full adder using half adder
4. Design a half subtractor circuit using gates and implement full subtractor by using half subtractor
5. Implementation of BCD adder using 4bit binary adders
6. BCD to excess- 3 code converter.
7. Design of binary to gray code converter
8. Design a 4X1 multiplexer and 1X4 Demultiplexer using logic gates
9. Design a 8X3 Encoder and 3X8 Decoder using gates
10. Design a simple 2-bit multiplier using half adders
11. Design a BCD to 7-segment decoder/driver
12. Implementation of 8 bit binary comparator using 4 bit binary comparators
13. Implementation of any two flip-flops using NAND & study of 7476
14. Implementation of shift register
15. Design of synchronous counter
16. Design of asynchronous counter

List of Augmented Experiments*

1. Design a Universal shift register.
2. Design a sequence detector
3. Design of ALU
4. Design a Digital Clock

Reading Material (s)

1. Morris Mano, Digital Design, PHI, 3rd Edition, 2001
2. Charles H. Roth, Fundamentals of Logic Design, Thomson Publications, 3rd Edition, 2014

* Students shall opt any one of the Augmented experiment in addition to the regular experiments

21ESX01 Employability Skills I

0 0 2 0

Course Outcomes

1. Demonstrate oral communication and writing skills as an individual to present ideas coherently
2. Develop life skills with behavioral etiquettes and personal grooming.
3. Assess analytical and aptitude skills.
4. Develop algorithms for engineering applications.
5. Solve engineering problems using software.
6. Utilize simulation tools for testing.

COs – POs Mapping

COs	PO1	PO2	PO5	PO8	PO10	PO12
1					3	2
2				1	2	2
3	2	1		2		
4	2		2			
5	2		2			
6	2		2			

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

1. Communication Skills, Confidence and Quantitative Aptitude

How Communication Skills affect Confidence? How to communicate effectively.(with Examples)

Listening: Listening?, Listening Vs Hearing, Possible reasons for why people do not Listen at times, Active Listening Vs Passive Listening, How Listening can affect our relationships? How Listening helps in Campus Placements also? (with Examples)

Goal Setting: SMART Technique to Goal Setting, Putting First things First, SWOT Analysis and Time Management

Attitude & Gratitude: Attitude Vs Skills Vs Knowledge, Attitude Vs Behaviour, How to develop Positive Attitude? Developing the attitude of Gratitude.

Public Speaking: JAM, J2M, Presentations by Students on General Topics.

7 Hours

2. Quantitative Aptitude

Number system, L.C.M and H.C.F, Problems on Ages, Averages, Time and work, Pipes and cisterns

8 Hours

Unit II

Verilog Language Constructs and Gate Level Modelling

Verilog as HDL, Levels of design description, Concurrency, Simulation and Synthesis, Functional verification, System tasks, Programming Language Interface (PLI), Module, Simulation and Synthesis tools, Test benches, Keywords, Identifiers, White space characters, Comments, Numbers, Strings, Logic values, Strengths, Data types, Scalars and Vectors, Parameters, Memory, Operators, System tasks, AND gate primitive, Module structure, Other gate primitives, Tristate gates, Array of instances of primitives, Delays, Strengths and Contention Resolution, Net Types, Design of basic circuits. Design of Flip-flops with Gate Primitives, adders, Parameters, Path delays, Module parameters, Hierarchical access

Practical Components

1. Introduction to EDA tool and Simulation of logic gates
2. Design and Simulate Full adder and Full Subtractor
3. Simulate the Flip-Flops using the Gate Primitives

15 Hours

Total 30 Hours

21HSX11 CC & EC Activities I

0 0 1 0

Course Outcomes

1. Interpret and present the abstractive technical information through an activity
2. Think critically in providing solutions to the generic and common problems
3. Demonstrate the creative thinking in dealing with liberal arts
4. Instill team sprit through active engagement with the peer
5. Develop programs of common interest having social impact
6. Empower the under privileged through motivational activities

COs –POs Mapping

COs	PO_6	PO_7	PO_9	PO_{10}
1				3
2	3	2		
3	3			
4			3	
5	3			
6	3			

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

21CSE01 Object Oriented Programming

3 0 0 3

Course Outcomes

1. Summarize object oriented programming concepts
2. Develop applications using different types of inheritances
3. Create simple applications using Interfaces, packages and collections
4. Analyse and recover runtime exceptions arise in the applications
5. Apply parallel processing applications using threads
6. Develop Interactive applications using AWT and Swing

COs–POs Mapping

COs	PO_1	PO_2	PO_5
1	3	2	1
2	-	-	-
3	3	1	2
4	-	-	-
5	1	1	2
6	-	-	-

3–Strongly linked | 2–Moderately linked | 1–Weakly linked

Unit I

Introduction to Java

Features of object oriented programming, Overview of Object Oriented Programming principles, Importance of Java to the Internet, Byte code, Methods, classes and instances, Data types, arrays, control statements, simple java program, Classes and Objects– constructors, methods, access control, this keyword, overloading methods and constructors, garbage collection, String handling methods and String Tokenizer.

Java History–Computer Programming Hierarchy–Role of Java Programmer in Industry **11 Hours**

Unit II

Inheritance, Packages & Interface

Inheritance: Basics, Using super, Multilevel Hierarchy, Method overriding, Dynamic Method Dispatch, Using Abstract classes, Using final with Inheritance.

Packages: Defining, Creating and Accessing a Package, Understanding CLASSPATH, importing packages, Member access rules.

Interface: Defining an interface, differences between classes and interfaces, implementing interface, variables in interface and extending interfaces, Nested–Inner Class & Anonymous Classes.

Generic Class Types **13 Hours**

Unit III

Exception Handling & Multithreading

Exception handling: Concepts and benefits of exception handling, exception hierarchy, usage of try, catch, throw, throws and finally, built-in and User Defined Exceptions.

Multithreading: Definition thread, thread life cycle, creating threads, synchronizing threads, daemon threads, Inter Communication of Threads.

Control Flow in Exceptions **11 Hours**

Unit IV

Event Handling

The AWT class hierarchy, user interface components labels, button, Text components

Event Handling: Events, Delegation event model, handling mouse and keyboard events, Adapter classes, inner classes, compare basic AWT components with swing components, more user interface components-canvas, scrollbars, check box, choices, lists panels–scroll pane, dialogs, menu bar, layout managers, *java.util Package.*

Anonymous Inner classes a Short–cut to Event Handling **13 Hours**

Total: 48 Hours

Textbook (s)

1. H. Schildt, Java: The complete reference, 8th Edition, TMH, 2011
2. T. A. Budd, An Introduction to Object–Oriented Programming, 3rd Edition, Addison Wesley Longman, 2002

Reference (s)

1. Dietal & Dietal, Java: How to Program, 8th Edition, PHI, 2010
2. C. Horstmann, BIG JAVA Compatible with Java 5 & 6, 3rd Edition, Wiley Publishers, 2008
3. C. S. Horstmann and G. Cornell, Core Java, Vol 1. Fundamentals, 7th Edition, Pearson Education, 2004

Sample Questions:

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	25	20	--
Understand	35	30	--
Apply	40	50	50
Analyze	--	--	--
Evaluate	--	--	--
Create	--	--	50
Total (%)	100	100	100

Remember:

1. List any four primitive data types supported in Java.
2. Define an Interface and write the syntax to create an Interface.
3. List any 4 features of Object Oriented Programming.
4. Write the syntax for anonymous class.

Understand:

1. Does java support multiple inheritance? If so, how it can be achieved?
2. What is meant by an Array in Java?
3. Write a program that demonstrates the single and two dimensional int and float Array.
4. What is the purpose of method overloading in Java?
5. Write a Java program that demonstrates the method overloading.

Apply:

1. Consider a banking application which consists of the following operations for an account: checkBalance(), deposit(), withdrawal() and interest(). Create a base class Account which consists of the above mentioned methods. Demonstrate the same application using Dynamic Method Dispatch concept by creating a subclass for SBI which should have minimum balance of Rs.1000.

2. Write an abstract class called Shape consists of area () and perimeter () as abstract methods. Derive subclasses named Circle, Triangle, and Rectangle from Shape class with area () and perimeter () implementation. Write a test program that create objects for Circle, Triangle, and Rectangle and print the corresponding area and perimeter.

Analyze:

1. Analyze the differences between classes, abstract classes and interfaces with suitable examples.
2. Analyze member access rules with respect to same class, same package subclass, same package non-subclass, different package subclass and different package non-subclass with a suitable program.

Create:

1. Gopal is an athlete, striving hard for his running competition and decides to practice well for it. He wants to track his speed and decides to maintain the time taken for him for each of his practice session. He now decides to buy a stopwatch and approaches you. Now, design a stopwatch for John to track time in terms of minutes and seconds. Add functionalities like Start, Reset and Pause for the stopwatch. Use Applets, AWT components and Threads and implement the stopwatch.

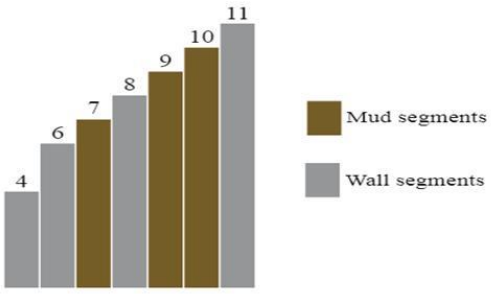
2.Your company is designing a dam to be built across a stream to create a small lake. To reduce materials cost, it will be made of one or more concrete walls with mud packed in between them. Determine the maximum height of the mud segments in the dam with the following restrictions:

One unit width of the gap between walls will contain one segment of packed mud
The height of mud in a segment cannot exceed 1 unit more than an adjacent wall or mud segment.

Given the placement of a number of walls and their heights, determine the maximum height of a mud segment that can be built. If no mud segment can be built, return 0.

Function Description
Complete the function maxHeight() which takes the following parameter(s):
int wallPositions[n]: an array of integers
int wallHeights[n]: an array of integers
Returns:
int: the maximum height mud segment that can be build
Constraints
$1 < n \leq 105$
$1 \leq$ wallPositions[i], wallHeights[i] ≤ 109 (where $0 \leq i < n$)

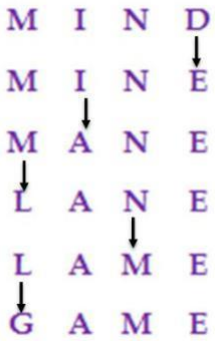
Example
wallPositions = [1, 2, 4, 7]
wallHeights = [4, 6, 8, 11]



- There is no space between the first two walls.
- Between positions 2 and 4, there is one unit open for mud. Heights of the surrounding walls are 6 and 8, so the maximum height of mud is 6 + 1 = 7.
- Between positions 4 and 7 there are two units. The heights of surrounding walls are 8 and 11.
- The maximum height mud segment next to the wall of height 8 is 9.
- The maximum height mud next to a mud segment of height 9 is 10.
- Overall, mud segment heights are 7, 9 and 10, and the maximum height is 10.

[Open Book Examination Question]

3. A word-ladder puzzle is one in which you try to connect two given words using a sequence of English words such that each word differs from the previous word in the list only in one letter position. For example, the figure below shows a word ladder that turns the word MIND into the word GAME using six single-letter steps.



Write a program that checks the correctness of a word ladder entered by the user. Your program should read in a sequence of words and make sure that each word in the sequence follows the rules for word ladders, which means that each line entered by the user must

- Have the same number of characters as the preceding word
- Differ from its predecessor in exactly one character position.

All words being assumed to be in upper case. If the user enters a word that is not legal in the word ladder, your program should print out a message to that effect and let the user enter another word. It should stop reading words when the user enters a blank line. Thus, your program should be able to duplicate the following sample run that appears on the next page. **[Open Book Examination Question]**

21EC401 Analog and Digital Communications

3 0 0 3

Course Outcomes:

1. Explain Analog Modulation & Demodulation techniques
2. Summarise the noise level in Analog communication systems
3. Demonstrate the operations of Transmitters and Receivers
4. Explain different pulse modulation techniques
5. Illustrate different digital modulation and demodulation techniques
6. Outline the operations of digital communication receivers

COs-POs Mapping

COs	PO_1	PO_2	PSO_2
1	2		2
2	2		2
3	3	2	3
4	2		2
5	2		2
6	3	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Amplitude Modulation and Frequency Modulation

Introduction to communication system, Need for modulation, Frequency Division Multiplexing, Amplitude Modulation, power relations in AM waves, Generation of AM waves: square law Modulator, Principle of Detection of AM Wave: Envelope detector. DSB Modulation: Double side band suppressed carrier modulators, Generation of DSBSC Waves, Coherent detection of DSB-SC Modulated waves.
SSB Modulated Wave, Vestigial side band modulation: Generation of VSB Modulated wave.
Frequency Modulation: FM Wave, Narrow band FM, Wide band FM, Generation of FM Waves, Direct FM, Detection of FM Waves: Balanced Frequency discriminator.
Switching modulator, COSTAS loop

13 hours

Unit II

Noise, Analog Transmitters and Receivers

Noise in DSB & SSB System Noise in AM System, Noise in Angle Modulation System, Threshold effect in Angle Modulation System, Pre-emphasis & de-emphasis AM Transmitter, FM Transmitter - Variable reactance FM Transmitter, Super heterodyne receiver, Comparison of FM and AM Receiver.
Phase modulated FM transmitter, Phase locked loop

11 hours

Unit III

Pulse modulation

PAM, PWM, PPM, Model of Digital Communication Systems, Digital Representation of Analog Signal, Certain issues in Digital Transmission, Advantages of Digital Communication Systems , Pulse Code Modulation: PCM Generation and Reconstruction, Quantization noise, Non uniform Quantization and Companding, Time Division Multiplexing, DPCM, DM and Adaptive DM.
Classification of line encoding techniques, TDM Frame Structures

12 hours

Unit IV

Digital Modulations

Introduction, ASK, FSK Modulator, Coherent ASK Detector, Non-Coherent ASK Detector, FSK, Bandwidth and Frequency Spectrum of FSK, Non coherent FSK Detector, Coherent FSK Detector, BPSK, Differential PSK DEPSK, QPSK, MPSK, MSK, Probability of Error, Correlation Receiver, Matched filter Receiver.
Telemetry, OQPSK

12 hours
Total: 48 hours

Textbook (s)

1. H.Taub and D. Schilling, Principles of Communication Systems, TMH,4th Edition, 2017
2. Simon Haykin , Digital communications, John Wiley, 4th Edition,2013
3. Simon Haykin , An Introduction to Analog& Digital Communications, John Wiley, 2nd Edition, 2012
4. George Kennedy and Bernard Davis , Electronic Communication Systems, TMH, 4th Edition, 2004

Reference (s)

1. R.P. Singh, SP Sapre, Communication Systems TMH, 3rd Edition, 2017
2. B.P.Lathi, Zhi Ding, Modern Digital and Analog Communication Systems, Oxford, 4th Edition, 2011
3. John G. Proakis, Masond, Salehi, Fundamentals of Communication Systems, Pearson Education, 3rd Edition, 2008
4. H Taub & D. Schilling, Gautam Sahe, Principles of Communication Systems , TMH, 3rd Edition. 2007
5. Sam Shanmugam, Digital and Analog Communication Systems, John Wiley, 2005
6. Bernard Sklar, Digital communications Fundamentals and applications, 2nd Edition, PHI, 2001

Sample Question (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	25	25	--
Understand	50	50	--
Apply	25	25	80
Analyse	--	--	20
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. Define angle modulation.
2. Define modulation index.
3. List any two advantages of DSBSC.
4. List any two advantages of VSB.
5. Define quantization noise power.
6. Define QAM, and draw its constellation diagram.

Understand

1. Explain the need for modulation.
2. Illustrate the operation of square law modulator.
3. Compare SSB modulation with DSB-SC modulation.
4. Illustrate the operation of Frequency modulation.
5. Represent a neat block diagram of a typical digital communication system and explain the function of the key signal processing blocks.
6. Explain Binary PSK and QPSK with corresponding equations and constellation diagrams.

Apply

1. The antenna current of an AM transmitter is 8A when only the carrier is sent, but it increases to 8.93A when the carrier is modulated by a single sine wave. Calculate the percentage modulation. Find the antenna current when the percentage of modulation changes to 0.8.
2. An FM signal with single tone modulation has a frequency deviation of 15KHz and a bandwidth of 50KHz. Find the frequency of the modulating signal.
3. Execute the channel synchronization method in PCM systems.
4. A standard AM broad cast station is allowed to transmit 12 signals ,each band limited to 5KHz and are to be transmitted over a single channel by FDM. If AM –SSB modulation with guard band of minimum

value is used, Find the band width of the multiplexed signal. Predict the number of signals can be used if AM-DSBSC is used by the broad cast station instead of AM-SSB for the same bandwidth.
[Open Book Examination Question]

5. a)A QPSK signal is used to send data over a satellite transponder. The transponder has a bandwidth of 12MHz.A TV channel is planned to use two data rates of 18MHz and 28MHz.Find which data rate can be supported by the transponder and Justify the reason.
   b) For the same transponder ,Find whether the TV channel can use the data rates of 15MHz and 30 MHz or not.
   [Open Book Examination Question]

Analyse

1. Certain transmitter is radiating 132KW when a certain audio sinewave is modulating it to a depth of 80% and 150KW when a second sinusoidal audio wave also modulates it simultaneously. What is the depth of modulation for the second audio wave?
2. When the modulating frequencies in an FM system is 400Hz and the modulating voltage is 2.4v the modulation index is 60. What is the modulation index when the modulating frequency is reduced to 250 Hz and the modulating voltage is simultaneously raised to 3.2V Calculate the maximum deviation.
3. Outline the signal space diagram of quadrature amplitude modulation and its differences with respect to QPSK. Analyze different ways of increasing the efficiency of steam power plant by giving appropriate justification.
4. a) An All India radio station uses a carrier wave of 1MHz and whose amplitude is 3V is frequency modulated by a sinusoidal modulating signal frequency of 500Hz and of peak amplitude 1V.The peak deviation of the modulating wave form is 1KHz.The peak level of the modulating waveform is changed to 5V and the modulating frequency changed to 2KHz.Then find the expression for the new modulated wave and compare the parameters such as deviation ratio, Bandwidth and the number of side bands of FM waves.
   b) In the radio station if the carrier wave is changed to a square wave for the same specifications find the expression of the modulated wave and compare the parameters of the FM waves with sine and square modulating signals.
   [Open Book Examination Question]

5. a) In a music competition, recording is done by sampling and storing the sample values .If the highest frequency tone to be recorded is 15800Hz, Examine the number of sample would be required to store
   three minutes performance. Conclude the number of binary digits would be required to store the three minutes performance if each sample is quantized in to 128 levels.
   b)Find the number of binary digits required to store 5 minutes performance if each sample is quantized in to 64 levels.
   [Open Book Examination Question]

21EC402 Analog Electronic Circuits

3 0 2 4

Course Outcomes

1. Design Sinusoidal oscillators for a given frequency
2. Outline the feedback amplifiers and power amplifiers
3. Explain the operation of tuned amplifiers used in communication systems
4. Construct linear & nonlinear wave shaping circuits for given application
5. Design Multivibrator for a given frequency
6. Summarize different Time base circuits

COs –POs Mapping

COs	PO_1	PO_2	PO_4	PO_5	PSO_1
1	3	2	2	3	3
2	3	3	2	3	3
3	2				2
4	3	2	2	3	3
5	3	2	2	3	3
6	2				2

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Feedback Amplifier & Sinusoidal Oscillators

Feed Back amplifiers - Concept of feedback, Effect of negative feedback on the amplifier characteristics, Topologies, Voltage Series, Current Series, Voltage Shunt and Current Shunt feedback Amplifiers.

Oscillators- Condition for oscillations, Hartley oscillator, Colpitts oscillator, RC phase shift oscillator, Wein bridge Oscillator, Crystal Oscillator.

Clapp oscillator, Tuned collector oscillator, Stability of oscillators

Practical Components

1. Design and simulate current series feedback amplifier and observe its frequency response.
2. Design and simulate Hartley oscillator for given frequency and observe the desired output waveforms.
3. Design and simulate RC phase shift oscillator for given frequency and observe the desired output waveforms.
4. Design and simulate the Wein bridge oscillator for a given frequency and observe the desired output waveforms.

13+ 8 Hours

Unit II

Power Amplifiers & Tuned Amplifiers

Class A power amplifier, Efficiency of Class A power amplifier - Resistive load, Transformer load, Class B power amplifier- Efficiency of Class B power amplifier- Push Pull, Complimentary Symmetry, Class C power amplifier, Class D power amplifier.

Single Tuned Capacitive Coupled Amplifier - Quality factor of a tank circuit, Gain & Bandwidth, Stagger tuned amplifiers,

Application of Tuned Amplifiers, Neutralization techniques

Practical Components

1. Simulate a Class A resistive load amplifier and find the efficiency.
2. Simulate a Class A transformer load amplifier and find the efficiency.
3. Observe the frequency response of a single-tuned amplifier.
4. Observe the frequency response of a stagger-tuned amplifier.

12+ 8 Hours

Unit III

Linear & Non Linear Wave Shaping Circuits

Response of High pass & Low pass RC circuits with sinusoidal, step, pulse, square inputs. RC network as differentiator and integrator, Attenuators.

Diode clippers, Transfer characteristics of clippers, Comparators, Clamping operation, clamping circuits using diode with different inputs, Clamping circuit theorem.

Double differentiator, Applications of voltage comparators

Practical Components

1. Design and simulate a high-pass RC circuit for square wave input and observe the response.
2. Design and simulate a low-pass RC circuit for square wave input and observe the response.
3. Design and simulate different types of clipping circuits for given sinusoidal input and observe the desired output waveforms.
4. Design and simulate different types of clamping circuits for a given input and observe the desired output waveforms.

12+8 Hours

Unit IV

Non Sinusoidal Waveform Generators

Collector coupled Astable Multivibrator, Monostable Multivibrator, Bistable Multivibrator, Schmitt Trigger. General features of a time base signal, Voltage sweep generators using UJT, Miller and Bootstrap time base generators, Current time base generators.

Application of Multivibrator, Applications of Time base generators

Practical Components

1 Simulate the Astable multivibrator and observe the desired waveforms at each base and Collector.
2 Simulate the Monostable multivibrator and observe the desired waveforms at each base and Collector.
3 Simulate the Bistable multivibrator and observe the desired waveforms at each base and Collector.
4 Design and simulate UJT Relaxation Oscillator to generate time base signal.

11+8 Hours

Total : 48+32 Hrs

Textbook (s)

1. J.Millman, C.C.Halkias and Chetan D Parikh, Integrated Electronics, 2ndEdition, Tata McGraw Hill, 2017
2. A. Anand Kumar, Pulse and Digital Circuits, PHI, 2005

Reference (s)

1. K.Venkata Rao, K.Rama Sudha, Electronic Devices and Circuits, McGraw Hill, 1st Edition, 2015
2. VenkataRao.K, RamaSudha.K and Manmadha Rao.G, Pulse and Digital Circuits, Pearson Education, 1st Edition, 2012
3. Robert L. Boylestad and Louis Nashelsky, Electronic Devices and Circuits Theory, Pearson/Prentice, 11th Edition, 2012
4. J. Millman, H. Taub and M. Surya Prakash Rao, Millman's Pulse, Digital and Switching Waveforms, McGraw-Hill, 3rd Edition, 2010
3. M.H. Rashid, Thomson, Micro Electronic Circuits: Analysis and Design, PWS Publishers,1999

Sample Question (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Lab Examination (%)
Remember	20	20	--
Understand	40	40	--
Apply	40	40	100
Analyse	--	--	--
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	--

Remember

1. Define characteristics of negative feedback amplifiers.
2. Define barhausian criteria.
3. Define Linear wave shaping circuits.
4. Define slope, displacement and transmission errors in voltage sweep generators.
5. State clamping circuit theorem.

Understand

1. Explain the operation of Hartley oscillator? Derive the expression for frequency of oscillation.
2. Illustrate the operation of crystal oscillator with equivalent circuits.
3. Compare positive and negative feedback amplifiers.
4. Illustrate the response of High pass RC circuit to square wave input.
5. Explain the working of boot strap time base generator with transistor.

Apply

1. Compare the performance of Class A and class B amplifier.
2. Draw the practical circuit of current series and voltage series negative feedback amplifier.
3. Show a high pass circuit having a time constant smaller than the time period of input signal behaves as a differentiator.
4. Design a symmetric collector-coupled astable multivibrator to genereate the square wave of 10 kHz having peak to peak amplitude 10V where hfe(min)=30, Ic=2mA.
5. Design a Schmitt trigger circuit for the following specifications: UTP=8V,LTP=5V, Vcc =15V, hfe=25 and Ic =2mA.

21EC403 Electromagnetic Fields and Waves

3 0 0 3

Course Outcomes

1. Classify different coordinate systems
2. Compare different charge distributions using Coulomb's law & Gauss law
3. Compute the charge and current distributions of electrostatic and magneto static fields
4. Illustrate Maxwell's equations for plane waves and their propagation in different media
5. Formulate reflection and refraction coefficients of uniform plane waves in different media interfaces
6. Differentiate wave equations for medium

COs – POs Mapping

COs	PO_1	PO_2	PSO_2
1	2		2
2	2		2
3	3	2	3
4	2		2
5	2		2
6	3	3	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Vector calculus and coordinate systems

Vector fields–Different co-ordinate systems, Physical significances of grad, div, curl. Line integral, surface integral, volume integral- physical examples in the context of electricity and magnetism and statements of Stokes theorem and Gauss theorem. Expression of grad, div, curl and Laplacian in Spherical and Cylindrical co-ordinates.

Differential surface and differential volumes in cylindrical and spherical system

10 Hours

Unit II

Electrostatics

Experimental Law of Coulomb, Electric Field Intensity, Fields due to Continuous charge distributions - Line Charge, Ring of charge and Sheet Charge. Electric Flux Density, Gauss' Law, Gauss' Law Differential form, Applications of Gauss' Law. Work done in Moving a Point Charge in an Electric Field, Line Integral, Definition of Potential, Calculation of potential differences for different configurations. Relation between E & V, Energy Density in static Electric Field, Poisson's and Laplace's Equations.

Capacitance evaluation for parallel plate, coaxial and spherical capacitors

14Hours

Unit III

Magnetostatics and Maxwell's equations

The Steady Magnetic Field: Biot-Savart Law, Ampere's Circuital Law and its Applications, Magnetic Flux and Flux Density, Scalar and Vector Magnetic Potentials, Force on a Moving Charge and Differential Current Element, Energy in Static magnetic fields, Basic expressions for self and mutual inductances.

Maxwell's Equations: Faraday's Law, Inconsistency of Ampere's law, Displacement Current, Maxwell's Equation in Point and Integral Form of different media, Boundary Conditions : Dielectric–Dielectric boundary, Dielectric–conductor boundary.

Inductance evaluation for solenoid and torpid

12 Hours

Unit IV

Uniform Plane Waves

Wave equations for conducting and Perfect Dielectric, Relation between E & H, Wave Propagation in lossless and conducting media, Good Conductors and Good Dielectrics, Skin Effect, Poynting Vector and Power Considerations, Wave Polarization.

Reflection and Refraction of Uniform Plane wave: Definitions of Reflection coefficient and Transmission coefficient, Waves at Normal Incidence for perfect conductor-dielectric boundary & dielectric-dielectric

boundary, Oblique incidence: Perpendicular and Parallel Polarization, for dielectric-dielectric boundary, Brewster angle.
Time harmonic fields, Complex Poynting vector

12 Hours
Total: 48 Hours

Textbook (s)

1. Matthew N.O. Sadiku, Elements of Electromagnetics, Oxford Univ. Press, 3rd Edition., 2001
2. William H. Hayt Jr. and John A. Buck ,Engineering Electromagnetics, Tata McGraw Hill, 8th Edition, 2001

Reference (s)

1. Gottapu Sasibhushana Rao, Electromagnetic Field Theory and Transmission Lines, Wiley Publishers, 1st Edition, 2012
2. G.S.N. Raju ,Electromagnetic Field Theory and Transmission Lines, Pearson Education, 1st Edition, 2006
3. Joseph Edminister ,Electromagnetics, Schaum Outline Series, McGraw Hill, 2nd Edition,1994
4. David K. Cheng, Field and Wave Electromagnetics, Pearson Education Asia, 2nd Edition.,1989, Indian Reprint 2001

Sample Question (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	20	20	--
Understand	55	55	--
Apply	25	25	60
Analyse	--	--	40
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. List co-ordinate systems.
2. State Gauss Law.
3. State Stokes theorem.
4. State Coulomb's law.
5. List the four Maxwell's Equations.
6. Define Uniform Plain Wave.
7. Define Vector Magnetic Potential.

Understand

1. Illustrate the significances of gradient, divergence, curl.
2. Explain Four point charges each 20μC are on x and y axis at ±4 m. Find the force on a 100μC point charge at (0,0, 3)m.
3. Illustrate ampere's law.
4. Formulate the relationship between unit vectors of Cartesian and Cylindrical Coordinates.
5. Formulate the Electric field intensity due to a circular disc of charge density ρs C/m^2 .
6. Explain Skin Effect.
7. Explain Wave Polarization.

Apply

1. A circular ring of charge with radius 2m, lies in z = 0 plane with center at origin. The charge density on the ring is 10nC/m. Find the point charge q at the origin which produces the same electric field at (0, 0, 5)m on that of the ring at the same point.
2.Two extensive homogeneous isotropic dielectric meet on plane for z>0

$\varepsilon_{r1} = 4$ and for z<0 , $\varepsilon_{r2} = 3$. A uniform electric field $\boldsymbol{E_1} = 5\boldsymbol{a_x} - 2\mathbf{a_y} + 3\mathbf{a_z}$ KV/m exists for $z \geq 0$. Find (i) $\boldsymbol{E_2}$ for $z \leq 0$ (ii) The energy densities (in J/m^3) in both dielectrics (iii) The energy within a cube of side 2m centered at (3,4,-5).

3. Given a uniform plane wave in air as

$\boldsymbol{E_i} = 40\cos(wt - \beta z)\,\boldsymbol{a_x} + 30\sin(wt - \beta z)\boldsymbol{a_y}$ V/m

(i)Find $\boldsymbol{H_i}$ and if the wave encounters a perfectly conducting plate normal to the z axis at z=0 an also find reflected wave $\boldsymbol{H_r}, \boldsymbol{E_r}$.

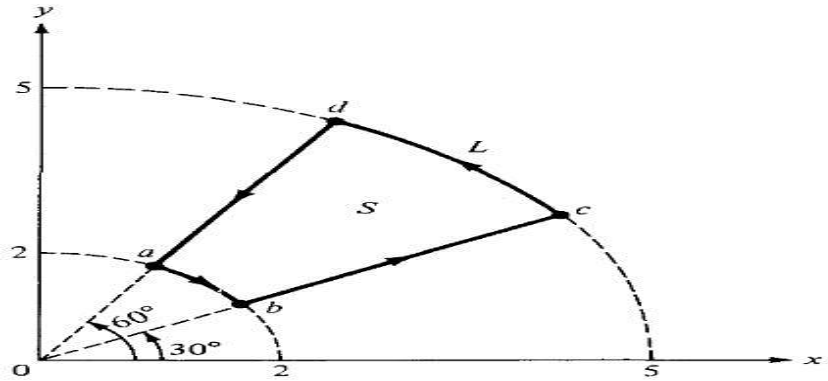
(ii**)**What are the total E and H fields for $z \leq 0$ and calculate the time average pointing vectors for$z \leq 0$ and $z \geq 0$.

4. Determine **D** at (4, 0, 3) if there is a point charge -5π mC at(4,0,0) and a line charge 3π mC/m along y axis.
5. Find the energy in the system for three different point charges $-1nC, 4nC$ $and 3nC$ are located at (0.0, 0), (0,0,1) and (1,0,0) respectively.
6. You are given four slabs of lossless dielectric, all with the same intrinsic impedance, ŋ, known to be different from that of free space . The thickness of each slab is ʎ/4 , where ʎ is the wavelength as measured in the slab material. The slab are to be positioned parallel to one another, and the combination lies in the path of a uniform plane wave , normally incident . The slabs are to be arranged such that the air spaces between them are either zero, one –quarter wavelength, or one – half wavelength in thickness. Specify an arrangement of slabs and air such that: (a) The wave is totally transmitted through the stack.
   (b) The stack present the highest reflectivity to the incident wave. Several answers may exist.
   [Open Book Examination Question]

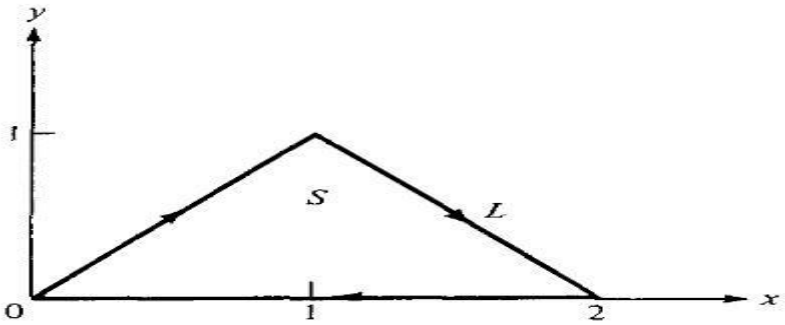
7. An empty metal paint can is placed on a marble table , the lid is removed , and both parts are discharged by touching to ground . An insulating nylon thread is glued to the center of the lid and a penny, a nickel and a dime are glued to the thread so that they are not touching each other. The penny is given a charge of +5nC and the nickel and dime are discharged. The assembly is lowered into the container so that the coins hang clear of all walls, and the lid is secured. The outside of the container is again touched momentarily to ground. The device is carefully disassembled with insulating gloves and tools. (a) What charges are found on each of the five metallic pieces? (b) If the penny had been given a charge of +5nC, the dime a charge of -2nC, and the nickel a charge of -1nC, what would the final charge arrangement have been?
   [Open Book Examination Question]

Analyse

1. If $\mathbf{A} = \rho\cos\phi\,\boldsymbol{a_z} + sin\phi\boldsymbol{a_\phi}$ evaluate $\oint \boldsymbol{A}.\boldsymbol{dl}$ around the path as shown in figure , and confirms this by using stokes theorem



2. Given that $\mathbf{F} = x^2\mathrm{y}\,\mathbf{a_x} - \mathrm{y}\,\mathbf{a_y}$ Find the $\oint \boldsymbol{F}.\boldsymbol{dl}$ around the path L as shown in figure and confirm the result by Stokes theorem.



3. Determine the flux of $\mathbf{D} = \rho^2 \cos\phi^2 \, \boldsymbol{a}_\rho + z \, sin\phi \boldsymbol{a}_\phi$ over the closed surface of the cylinder $0 \le z \le 1, \rho = 4$. Verify the divergence theorem for this case.

4. A charge distribution with spherical symmetry has density

$$\rho_v = \begin{cases} \frac{\rho_o r}{R} & 0 \le r \le R \\ 0, & r > R \end{cases}$$

Determine **E** everywhere.

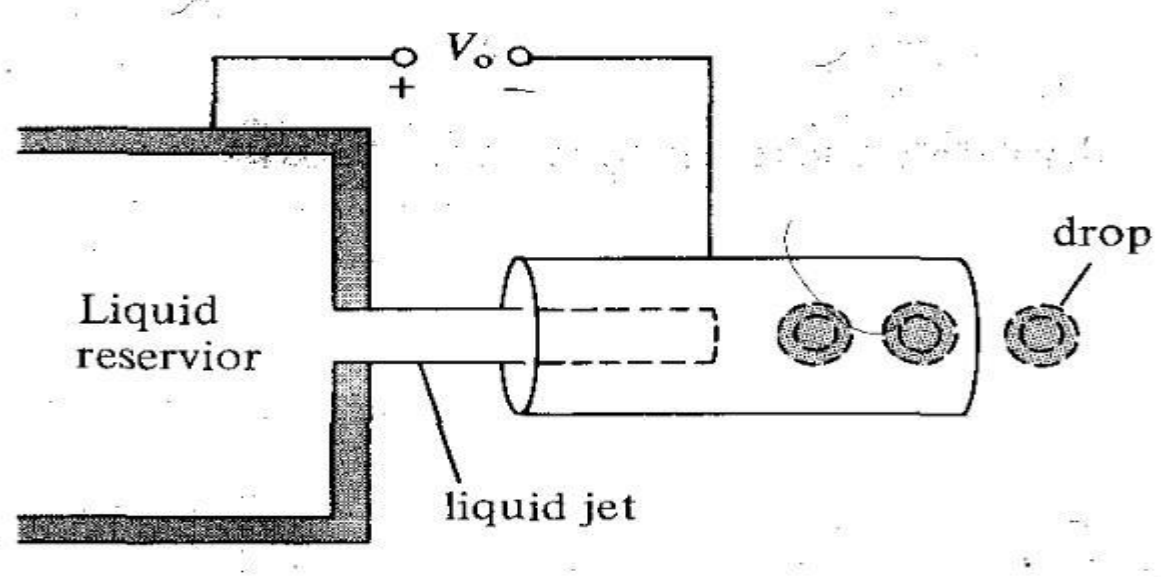
5. The electric field and, magnetic field in space are

$$E = \frac{50}{\rho} \cos(10^6 \, t + \beta z) \, \boldsymbol{a}_\emptyset \text{ V/m}$$

$$H = \frac{H_o}{\rho} \cos(10^6 \, t + \beta z) \, \boldsymbol{a}_\rho \text{ A/m}$$

Express these in phasor form and determine the constants $H_o \; and \; \beta$ such that the fields satisfy Maxwell's equation.

6. In an ink-jet printer the drops are charged by surrounding the jet of radius 20 μm with a concentric cylinder of radius 600 μm as show in figure . Calculate the minimum voltage required to genarate a charge 50 fC on the drop if the lengh of the jet inside the cylinder is 100 . Consider $\varepsilon = \varepsilon_{0 = 0}$

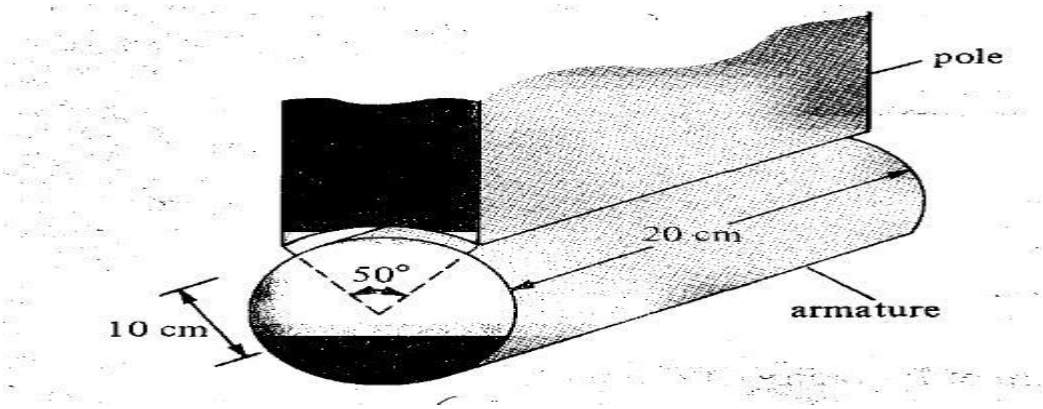


[Open Book Examination Question]

7. The electric motor shown in figure has filed

$$H = \frac{10^6}{\rho} \sin 2\emptyset \, a_\rho \text{ A/m}$$

Calculate the flux per pole passing through the air gap if the axial length of the pale is 20cm



[Open Book Examination Question]

21EC404 Linear Control Systems

3 0 0 3

Course Outcomes

1. Identify openloop and closed loop control systems and formulate the mathematical model
2. Interpret block diagram representation and signal flowgraph of control system
3. Demonstrate time response of system, Routh-Hurwitz , and rootlocus stability criterion
4. Illustrate the stability of a system using frequency domain techniques
5. Design different compensators and controllers in time/frequency domain
6. Outline the state space modeling of physical systems

COs – POs Mapping

COs	PO_1	PO_2	PSO_1	PSO_2
1	2		2	2
2	2		2	2
3	3	2	3	3
4	2		2	2
5	3	2	3	3
6	3	3	3	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Mathematical Models Of Physical Systems

Concepts of Control Systems- Open Loop and closed loop control systems, Classification of control systems, Modeling of Electric systems, Translational and rotational mechanical systems, Block diagram reduction technique, Signal flow graph, Mason's gain formula, Feedback Characteristics-Effects of feedback.

Effect of feedback on disturbance, Linearization of nonlinear mathematical models **11Hours**

Unit II

Time Domain Analysis

Standard test signals, Time responses of first order and second order systems, time domain specifications, characteristic Equation, Static error constants, Generalized error series, The concept of stability, Routh-Hurwitz stability criterion, Difficulties and limitations in RH stability criterion, Root locus concept, Construction of root
loci, Stability analysis using root locus, Effects of addition of poles and zeros on root locus. *Root loci for systems with transportation lag, Dominant closed loop poles* **13 Hours**

Unit III

Frequency Domain Analysis

Frequency response characteristics, Frequency domain specifications, Time and frequency domain parameters correlations, Bode plot, transfer function from the Bode plot, Stability Analysis using Bode Plot, Polar Plot, Nyquist's stability criterion, Effect of PI, PD, PID controllers, Lag, Lead, Lead-Lag Compensators design using Bode plot.

M & N circles, Nicholas Chart **14 Hours**

Unit IV

State Space Analysis

Concepts of state, state space modeling of physical systems, Representation of state space model in different canonical forms, Transfer function and state space model correlations, Solution of state equations, State Transition Matrix and it's Properties, Controllability and Observability.

Eigen vectors and Diagonalization **10 Hours**

Total: 48 Hours

Text Book (s)

1. I.J. Nagrath and M. Gopal, Control Systems Engineering, New Age International (P) Limited, 2nd edition, 2018
2. B. C. Kuo, Automatic Control Systems, John wiley and sons, 8th edition, 2014

Reference Book (s)

1. Norman. S. Nise, Control Systems Engineering, John wiley & Sons, 3rd Edition, 2018
2. K.Alice Mary and P.Ramana, Control Systems, Universities Press, 1st edition, 2016
3. Katsuhiko Ogata, Modern Control Engineering, Prentice Hall of India Pvt. Ltd., 3rd edition, 2015
4. Joseph J Distefano, Schaum's Series of Feedback and Control Systems, McGra Hill, 3rd edition, 2013

Sample Question (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	25	15	--
Understand	50	35	--
Apply	25	50	60
Analyse	--	--	40
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. Define a closed loop control system.
2. List any 4 applications of closed loop control system.
3. Define transfer function.
4. List 2 advantages of Signal flow graph over Block-diagram reduction technique.
5. List any 3 properties of state transition matrix.
6. Label different types of frequency domain analysis methods.
7. List the two advantages of Bode Plot.
8. Define Centroid.

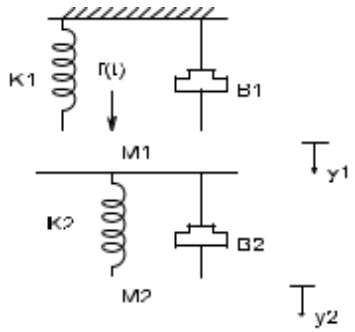
Understand

1. Compare SISO and MIMO systems.
2. Explain the traffic control system concepts using open loop as well as closed loop system.
3. Explain f-v and f-i analysis.
4. Explain different cases in R-H criteria.
5. Represent state transition matrix.
6. Explain Mason's gain formula.
7. Represent two difficulties in R-H Criteria and explain.
8. Compare and give correlation between time domain specifications and frequency domain specifications.

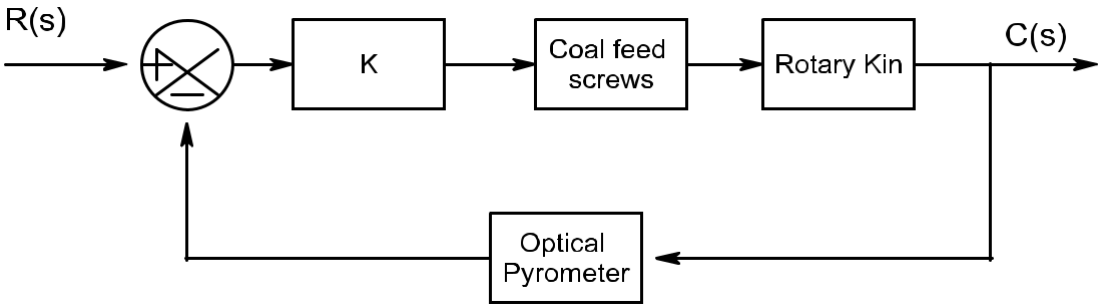
Apply

1. Find Open Loop and closed loop control systems for the person walking on a road.
2. Construct root locus for the open loop T.F function G(s) = (s+2)/(s+1)(s+3).
3. Construct the polar plot for a system having transfer function G(s)=1/s(s+1)(s+2) and find Gain margin and phase margin.
4. Demonstrate about Lead Compensator.
5. Demonstrate the Non homogenous solution for state equation.

6. For the mechanical translation system shown in the figure, find Y2(s)/F(s).



7. Cement is manufactured in large Rotary Kilns where raw lime stone is added and product clinker emerges after high-temperature processes. The clinker is later is cooled and estimated for its quality.The quality of clinker depends on many factors, one of the prime factor being the temperature in the burning zone. This temperature is sensed by an optical pyrometer. The temperature is maintained by manipulating the coal feed rate to the burners. This is accomplished by adjusting the speed of variable –speed coal feed screws. The model of control process is depicted in the figure.
Assume that the transfer function of clinkerization process is 1/(s + 1)(2s + 1) that of the sensor and
coal feed screw is unity. Find the value of K such that system is stable.



[Open Book Examination Question]

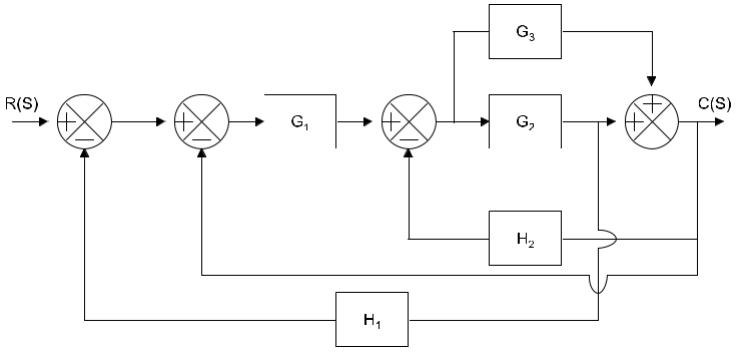
8. A unity feedback system is characterized by an open loop transfer function

$$G(s) = \frac{k}{s\,(s+10)}$$

Find the at least two methods to identify the stability of the system. Which method is more optimum. Justify your answer.
[Open Book Examination Question]

Analyze

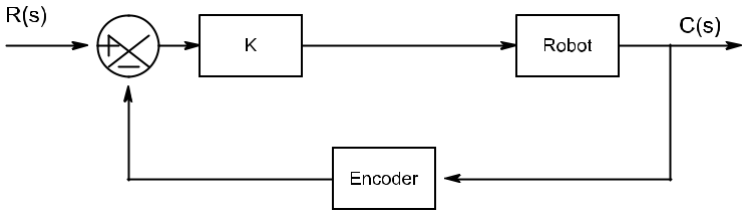
1. Resolve C(S)/R(S) using block diagram reduction rules for the given block diagram.



2. Outline the effect of disturbance on the system performance due to feedback.
3. Differentiate the advantage and disadvantages of the root locus and Bode plot.
4. Justify whether the following state space model is state controllable are not.

$$= \begin{bmatrix} -1 & 0 & 0 \\ 0 & -2 & 0 \\ 0 & 0 & -3 \end{bmatrix} B = \begin{bmatrix} 1 & 0 \\ 2 & 1 \end{bmatrix}$$

5. Outline the state space model in different canonical forms.
6. Outline the following transfer function $C(s)/R(s)=s^2+12s+8/s^3+9s^2+23s+8$ by controllable canonical form.
7. The position of an industrial robot manipulator used for welding in an automobile industry has to be controlled accurately. The position is maintained by a DC servo motor and the feedback is given by optical encoder. The block diagram of the process is given in figure.



A unity feedback system has transfer function of G(s) = 4/s(2s + 1) and the transfer unction of optical encoder is unity, analyze K value such that settling time is to be less than 0.5 sec and stability.

[Open Book Examination Question]

8. A unity feedback system has an open-loop transfer function of $G(s) = 4/s(2s + 1)$. It is desired to obtain a phase margin of 40o without sacrificing the Kv of the system. Find a suitable network to get the above. Justify your answer. Compute the value of network components.

[Open Book Examination Question]

21CSE02 Object Oriented Programming Lab

0 0 3 1.5

Course Outcomes

1. Make use of JAVA SDK environment to create - debug and run java programs
2. Create applications based on code reusability
3. Develop programs using threads
4. Develop and debug real time problems using exception handling
5. Using IDE, create interactive applications using event handling mechanisms
6. Design Graphical User Interface using AWT components and Swing

COs – POs Mapping

COs	PO_1	PO_2	PO_4	PO_5
1	1	3	3	1
2	2	3	3	1
3	3	2	2	1
4	2	2	3	1
5	3	2	3	2
6	3	2	2	2

3 – Strongly linked | 2 – Moderately linked | 1 – Weakly linked

List of Experiments

Students will perform minimum twelve Experiments

Write Java programs to:

1. Demonstrate the basics of Java using classes, methods and objects.
2. Develop a java program that print all real solutions to the quadratic equation ax2+bx+c=0
3. Demonstrate String handling methods.
4. Demonstrate this keyword in different ways
5. Demonstrate the different types of inheritance concept.
6. Demonstrate Inheritance concept using method overriding, super & final keywords and runtime polymorphism
7. Create a java Program to achieve multiple inheritance
8. Implement matrix operations using multidimensional arrays
9. Create a package which has classes and methods to read Student Admission details
10. Extracting tokens using StringTokenizer
11. Handle checked and unchecked exceptions using try-catch, finally, throw and throws keywords
12. Handle user-defined Exceptions
13. Develop a java program for thread Synchronization using by synchronized method and block.
14. Design a Job Application/ Student Admission Form and store the values in a file
15. Handle simple event to display cut/copy/paste events using Swings
16. Emulate the working of a simple Calculator.

List of Augmented Experiments

1. New Patient Registry Management System
2. Restaurant Billing Management System
3. Library Management System
4. ATM Management System
5. Bus Ticket Booking Management System
6. Movie Ticket Booking Management System
7. Queuing Management System
8. Attendance Management System
9. Medical Store Billing Management System
10. Text Editor Projects in Java
11. Google Search Engine Filter
12. Electronic voting System
13. Day Planner
14. Library management System
15. Personal Finance Management System

Reading Material (s)

1. JAVA Lab manual, Department of CSE and IT, GMR

* Students shall opt any one of the Augmented experiment in addition to the regular experiments

21EC405 Analog and Digital Communications Lab

0 0 3 1.5

Course Outcomes

1. Implement sampling theorem
2. Assess analog modulation & demodulation techniques
3. Demonstrate the pulse modulation techniques
4. Implement different Baseband modulation techniques
5. Implement different Digital modulation techniques
6. Contrast the design issues in a digital communication system

COs-POs Mapping

COs	PO_1	PO_2	PO_4	PO_5	PSO_2
1	3	2	2		3
2	3	2	2	3	3
3	3	2	2	3	3
4	3	2	2		3
5	3	2	2		3
6	3	3			3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

List of Experiments
Students will perform minimum twelve Experiments

1. Verification of Sampling Theorem
2. Amplitude Modulation & Demodulation
3. AM-DSB SC -Modulation & Demodulation
4. Design of envelope Detector
5. Frequency Modulation &Demodulation
6. Pulse Amplitude Modulation–Modulation& Demodulation
7. PWM, PPM -Modulation & Demodulation
8. Pre-emphasis & de-emphasis
9. Phase Locked loop(PLL)
10. Verify the operation of Time Division Multiplexing
11. Verification of Delta Modulator
12. Generation and Detection of pulse code modulation
13. Generation and Detection of Differential Pulse Code Modulation
14. Generation and Detection of ASK
15. Generation and Detection of PSK
16. Generation and Detection of of FSK

List of Augumented Experiments*

1. Design of AM receiver
2. Mobile Phone Detector
3. FM Transmitter
4. FM Receiver
5. HAM Radio Receiver

Reading Material(s)

1. Simon Haykin , Digital communications, John Wiley, 4th Edition, 2013
2. H.Taub and D. Schilling, Principles of Communication Systems, TMH, 4th Edition, 2017
3.John G. proakis, Masoundsalehi, Gerhard bakh ,Contempary communication system using MATLAB &Simulink,Thomson India publishers, 2007

* Students shall opt any one of the Augmented experiment in addition to the regular experiments

21ESX01 Employability Skills I

0 0 2 2

Course Outcomes

1. Demonstrate oral communication and writing skills as an individual to present ideas coherently
2. Develop life skills with behavioral etiquettes and personal grooming.
3. Assess analytical and aptitude skills.
4. Develop algorithms for engineering applications.
5. Solve engineering problems using software.
6. Utilize simulation tools for testing.

COs – POs Mapping

COs	PO1	PO2	PO5	PO8	PO10	PO12
1					3	2
2				1	2	2
3	2	1		2		
4	2		2			
5	2		2			
6	2		2			

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

1. Building Confidence

Fear? Steps to Overcoming the Fear of Public Speaking?

Self Esteem: Definition? Types of Self Esteem, Causes of Low Self Esteem, Merits of Positive Self Esteem and Steps to build a positive Self Esteem.

Group Discussions (Practice): GD? GD Vs Debate, Overview of a GD , Skills assessed in a GD, Dos & Don'ts, & Conducting practice sessions (Simple Topics).

Motivational Talk: Team Work: Team Vs Group? Stages in Team Building, Mistakes to avoid and Lessons to Learn (Through Stories or Can be a Case Specific)

8 Hours

2. Quantitative Aptitude

Percentages, Profit and loss, Mixtures and Allegations, Simple Interest, Compound Interest

7 Hours

Unit II

Behavioural Level Modelling

Operations and Assignments, Functional Bifurcation, Procedural constructs: Initial, Always, Assignments with delays, Wait, Multiple always blocks Designs at Behavioural level, Blocking and Non-blocking assignments, Case statement, Simulation flow, Conditional statements, and loops- if, if-else, repeat, for, while, forever, parallel blocks, force-release, Event, System Tasks, and Functions, File based tasks and Functions, Compiler directives, User-Defined Functions, Tasks and Primitives-Introduction, Function, Tasks, User- Defined Primitives (UDP)

Continuous assignment structures, Delays, and Continuous assignments, Assignment to Vectors, Operators,

Practical Components

1. Perform Behavioural model for multiplexer and demultiplexer
2. Perform Behavioural model for 8 to 3 priority encoders
3. Perform Behavioural model for 4-bit counter and shift register
4. Perform the simulation of parity bit generation using functions and tasks
5. Performa two-bit binary addition using functions and tasks
6. Perform the simulation of half adder and display the stimulus, response of system tasks- $monitor,$display,$monitoron, $monitorof, $stop, $finish

15 Hours

Total 30 Hours

21HSX11 CC & EC Activities I

0 0 1 1

Course Outcomes

1. Interpret and present the abstractive technical information through an activity
2. Think critically in providing solutions to the generic and common problems
3. Demonstrate the creative thinking in dealing with liberal arts
4. Instill team sprit through active engagement with the peer
5. Develop programs of common interest having social impact
6. Empower the under privileged through motivational activities

COs –POs Mapping

COs	PO_6	PO_7	PO_9	PO_{10}
1				3
2	3	2		
3	3			
4			3	
5	3			
6	3			

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

21EC501 Linear and Digital IC Applications

3 0 0 3

Course Outcomes

1. Illustrate the characteristics and internal structure of Operational amplifier
2. Classify various configurations of differential amplifiers
3. Differentiate linear and non-linear applications of operational amplifier
4. Design various types of analog filters
5. Outline the operation and applications of IC 555 time and PLL
6. Compute the working of various types of ADCs and DACs

COs – POs Mapping

COs	PO_1	PO_2	PSO_1
1	2	-	2
2	2	-	2
3	3	2	3
4	3	2	3
5	3	2	3
6	3	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Integrated Circuit

DC and AC analysis of dual input balanced output differential amplifier, Properties of other differential amplifier configurations, DC coupling and cascade differential amplifier stages, current mirror, Level Translator, Constant current Bias circuit. Integrated circuits classification, package types, Op-Amp Block diagram,741 OP-AMP ideal and practical, DC and AC characteristics, 741 OP-AMP and its features, frequency response of OP-AMP Frequency compensation technique.

Temperature ranges, FET input OP-Amps **13 Hours**

Unit II

Applications of OP-AMPS

Inverting and non-inverting amplifier, adder, subtractor, integrator, differentiator, difference amplifier, instrumentation amplifier, V-I converters, I-V converters , comparators, Schmitt Trigger, Multivibrators, square wave and Triangular wave generators, RC phase shift oscillator, Log and antilog amplifiers.

Buffers, precision rectifiers **11 Hours**

Unit III

Analog filters, 555 Timers and phase locked loop

Introduction, Butterworth filters-first order, second order LPF, HPF filters. Band pass, Band reject and all pass filters, Introduction to 555 Timer, functional diagram, Monostable and Astable operations and applications, Schmitt Trigger, VCO, PLL: Introduction, Block schematic, principles and description of individual blocks,565 PLL .applications of PLL: Frequency multiplication, frequency translation.

AM, FM and FSK demodulators using PLL. **12 Hours**

Unit–IV

D/A & A/D Converters, IC Regulators

Introduction, , Sample & Hold amplifiers, Weighted resistor DAC, R-2R Ladder DAC, Inverted R-2R DAC Parallel comparator type ADC, counter type ADC, successive approximation ADC and Dual slope ADC, IC regulators 78XX, 79XX, LM723,LM317, LM337, introduction to logic families (RTL, DTL, TTL, ECL).

DAC and ADC specifications **12 Hours**

Total: 48 Hours

Textbook (s)

1. Ramakanth A. Gayakwad, Op-Amps & Linear ICs, 3rd edition, PHI, 2002.
2. D. Roy Chowdhury, Linear Integrated Circuits, New Age International (p) Ltd, 2nd Edition, 2003.
3. Venkat Rao K, Rama Sudha K and Manmadharao G, Pulse and Digital Circuits, Pearson Education, 1st edition, 2012.

Reference (s)

1. Sergio Franco, Design with Operational Amplifiers & Analog Integrated Circuits, McGraw Hill, 2001.
2. Donald A Neamen, Electronic circuit analysis and design, Tata McGraw Hill, 2nd edition,2002.
3. R.F.Coughlin & Fredrick Driscoll, Operational Amplifiers & Linear Integrated Circuits, PHI, 6th edition, 2002.

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	10	20	--
Understand	30	30	--
Apply	30	40	60
Analyse		10	40
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. Define the non-ideal dc characteristics that add error components to the dc output voltage of Op-amp
2. The basic step of 9 bit DAC is 10.3mV. If 000000000 represents 0V, what output is produced if the input is 101101111?
3. List the ideal characteristics of operational amplifier
4. List the limitations of an ordinary Op-amp differentiator
5. List the components to assess the performance of R-2R ladder DAC

Understand

1. Classify differential amplifiers
2. Explain the operation of R-2R ladder DAC
3. Explain about the Op-Amp parameters that should be considered for AC and DC applications
4. Explain the working of a trans conductance amplifier with floating load using Op-amp
5. Compare different types of ADCs

Apply

1. Design a Practical differentiator that will eliminate the limitations of ordinary differentiator using op-amp
2. Design a Practical integrator that will eliminate the limitations of ordinary integrator using op-amp
3. Design a stable multivibrator using IC 555 and also determine its frequency
4. Design a filter to allow the signal frequency up to 2KHz
5. Design a R-2R ladder by using OP-AMP

[Open Book Examination Question]

Analyse

1. Design a Circuit which makes green bulb should be on for 4sec and red bulb should be on for 5sec alternatively by using 555 timer.
2. An Incubator is maintained at a temperature of 28^0c , design a circuit which will identify the variations in the temperature of incubator by using OP-Amp.
3. Design a Circuit to convert digital data streams into analog audio signals and compare which type of conversion DAC produce better results.
4. A differential amplifier has (i) CMRR = 1000 and (ii) CMRR = 10000. The first set of inputs is $v1$ = 100 μV and $v2$ = -100 μV. The second set of inputs is $v1$ = 1100 μV and $v2$ = 900 μV. Find the percentage difference in output voltages obtained for the two sets of input voltage and also comment on this
5. Design a circuit to identify the Male voice and separate the Female voice and convert the voice signal into a digital signal

   [Open Book Examination Question]

21EC502 Microprocessors and Microcontrollers

3 0 2 4

Course Outcomes

1. Summarize the architecture of 8086 microprocessor
2. Execute assembly language programs of 8086 microprocessor
3. Demonstrate the interfacing of peripherals with 8086 microprocessor
4. Explain the architecture of 8051 microcontroller
5. Implement assembly language programs of 8051 microcontroller
6. Carry-out the interfacing of peripherals with 8051 microcontroller

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PO_5	PSO_1
1	2	-	-	-	-	2
2	3	2	2	2	3	3
3	3	2	2	-	3	2
4	2	-	-	-	-	2
5	3	2	2	2	3	3
6	3	2	3	2	3	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

8086 Microprocessors and Assembly Language Programming

Introduction to microcomputer, evolution of processors and semiconductor memories (RAM, ROM, EPROM, EEPROM), Architecture of 8086 microprocessor, Register organization of 8086, Pipelining concept, Memory segmentation, Addressing Modes.

Instruction Set and Programming: Instruction set of 8086 microprocessor: Data transfer instructions, Arithmetic instructions, Logical Instructions, String instructions, Stack related instructions, Branching instructions, Assembler directives.

Data transfer instructions of 8085 microprocessor, Architecture of 8085 microprocessor

Practical Components

1. Data transfer program using different addressing modes in assembly language programming.
2. Perform arithmetic operations on 8 bit and 16 bit numbers in assembly language programming.
3. Data transfer program using string instruction in assembly language programming.
4. Program for data conversion in assembly language programming.

14+8 Hours

Unit II

8086 Operational Modes and Memory Interfacing

Minimum and Maximum mode operations of 8086 with timing diagrams, Procedures and macros, Stack Structure of 8086, Static RAM Interfacing, Interfacing of 8255 Programmable Peripheral Interface with 8086 microprocessor.

Dynamic RAM, Direct memory access

Practical Components

1. Write assembly language program using procedure.
2. Write assembly language program using macro.
3. Program to reject negative numbers from a series of bytes.

10+6 Hours

Unit III

8051 Microcontroller

Comparison between microprocessor and microcontroller, 8051 family microcontroller, RAM architecture of 8051, Integrated Development Environment (IDE), Pin description of 8051 microcontroller, Machine cycle. Addressing Modes, Instruction set of 8051: Data transfer instructions, Arithmetic instructions, Logical Instructions, Stack related instructions, Branching instructions. Programing and Applications of Timers, Interrupts, Universal Asynchronous Receiver Transmitter (UART).

External memory interfacing with 8051 microcontroller, various constituents of hex file

Practical Components

1. Perform Arithmetic operations on 8bit numbers in assembly language programming using 8051 microcontroller.
2. Program to toggle the LED.
3. Programming and interfacing of traffic light logic.
4. Program to generate square wave using interrupts.

12+8 Hours

Unit IV

Interfacing with 8051 microcontroller with External Peripherals

Interfacing with 8051 microcontroller with: Keypad matrix, LCD, Seven segment displays, L293D Motor driver, Stepper motor, Analog to Digital Converter (804), Digital to Analog Converter (808), introduction to CISC architecture, RISC architecture and ARM processor.

Interfacing of temperature sensor (LM 35) with 8051, interfacing of relay with 8051

Practical Components

1. Programming and interfacing of the key pad matrix.
2. Programming and interfacing of seven-segment display.
3. Programming and interfacing of the LCD.
4. Programming and interfacing of the relay.
5. Programming and interfacing of the dc/Stepper motor.

12+10 Hours

Total: 48+32 Hours

Textbook (s)

1. A.K. Ray & K. M Bhurchandi, Advanced Microprocessors & peripherals, Tata McGraw-Hill, 3rd Edition, 2012
2. Muhammad Ali Mazidi, Janice Gillispie Mazidi and Rolin D. McKinlay, The 8051 Micro controller and Embedded systems: using assembles and C, Pearson, 2nd Edition,2007

Reference (s)

1. D.V.Hall, Microprocessor and Interfacing, Tata McGraw Hill Publishing Company, 2nd Edition 2006
2. N. Sentil Kumar, M Sarvanan, S Jeevananthan, Microprocessors and Microcontrollers, Oxford University Press, 1st Edition, 2010
3. Kenneth J Ayala, The 8051 Microcontroller Architecture, Programming and Applications, Thomson Publishers, 3rd Edition, 2004

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Lab Examination (%)
Remember	25	25	--
Understand	35	35	--
Apply	40	40	100
Analyze	--	--	--
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. List out any four sixteen bit registers of 8086 microprocessor which can't split into two eight bit registers.
2. State the advantages of memory segmentation.
3. State the significance of Reset pin of 8051 microcontroller.
4. List four differences between 8051 family of microcontroller.

Understand

1. Calculate the physical address generated by the 8086 microprocessor to fetch the code if CS = A40H & IP = AAAAH.
2. Explain the function of BIU and EU of 8086 microprocessor.
3. Explain the consequences of execution of MOV IP, #14H instruction of 8051 microcontroller.
4. Explain the structure of internal RAM of 8051 microcontroller.
5. Explain the significance of each bit of TMOD register of 8051 microcontroller.

Apply

1. Write a program for 8051 microcontroller in assembly language to generate a square wave of 10KHz from pin P2.1. Assuming frequency of crystal attached to the microcontroller is 12MHz.

2. Develop a program in assembly language for 8051 microcontroller using interrupt to generate a 10KHz square wave from pin P2.0 and 25KHz square wave from pin P2.1 of 8051 microcontroller. Make suitable assumptions.
3. Interface a seven-segment display with 8051 microcontroller and develop a program in assembly language to display even numbers from 0 to 9.
4. Interface a LCD with 8051 microcontroller and develop a program in assembly language to display a message in 1st row of LCD.

21EC503 VLSI Design

Course Outcomes **3 0 2 4**

1. Explain the basic MOSFET circuits operation and MOS fabrication Process
2. Implement the layout diagrams for CMOS circuits
3. Assess the effects of parasitics and Scaling of MOS circuits
4. Interpret the operation of basic analog and digital MOSFET circuits
5. Implement the Digital and Analog circuits with Full-custom and Semi-custom design flows.
6. Interpret the VLSI implementation flows and the basics of VLSI testing

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PO_5	PSO_1
1	2	-	-	2	3	2
2	3	2	2	2	3	3
3	3	2	2	2	3	3
4	2	-	-	2	3	2
5	3	2	2	2	3	3
6	2	-	-	2	3	2

3–Strongly linked | 2–Moderately linked | 1–Weakly linked

Unit I

Introduction and basic electrical properties of MOS circuits: Introduction to VLSI Design Flow, Introduction to IC technology, I_{ds} versus V_{ds} Relationships, Aspects of MOS transistor Threshold Voltage, MOS transistor conductance, Output Conductance and Figure of Merit. Fabrication process: nMOS, pMOS and CMOS. Alternate pull up forms in inverter circuits, Pull-up to Pull-down Ratio for nMOS inverter driven by another nMOS inverter, basic current mirror, CMOS Inverter, Latch-up in CMOS circuits.
Static power dissipation, Dynamic Power dissipation in CMOS circuits

Practical components

1. Simulation of nMOS inverter
2. Functional verification of CMOS inverter
3. Functional verification of AND gate using pass transistor
4. Perform the simulation of the basic current mirror

13+8 Hours

Unit II

Basics of VLSI: Driving large capacitive loads, Cascaded CMOS inverters for delay optimization, Wiring Capacitances, Stick Diagrams, Design Rules and Layout, Layout Diagrams for MOS circuits, Sheet resistance, Gate capacitance, The Delay Unit, Inverter Delays, Scaling models and scaling factors, Scaling factors for device parameters, Limitations of scaling: performance improvement by CMOS scaling.
Drain Induced Barrier Lowering (DIBL) effect, Sub threshold conduction

Practical components

1. Layout design of CMOS inverter
2. Perform the DRC and LVS for the CMOS inverter Layout
3. Perform the RC extraction for CMOS inverter
4. Compute the delay of CMOS inverter after the RC extraction

11+8 Hours

Unit III

Basic Digital and Analog Circuits: Static CMOS logic, Cascode Voltage Switch Logic, Transmission Gates, Pass Transistor Logic, Dynamic logic, Domino logic, Metastability, setup time, hold time, Small signal Modeling of transistor, body bias effect, biasing styles of MOSFET FET amplifiers, single stage amplifier with resistive load, Common Source amplifier, Common Drain amplifier, Common Gate amplifier.
CMOS full adder, Clocked CMOS registers

Practical components

1. Design and simulation of Half adder using transmission gate logic
2. Simulate a one transistor Common Source amplifier with resistive load
3. Design and simulation of Half adder using pass transistor
4. Simulate a one-transistor common drain amplifier

12+8 Hours

Unit IV

VLSI Implementation Strategies and Testing:

Introduction, ASIC Design flow, types of ASICs- Full custom, Standard cell based Asics, Gate array based ASICs, FPGAs, FPGA design flow, Basic FPGA Design Structure FPGA Programming Technologies: SRAM, EPROM, EEPROM; Introduction to testing, Manufacturing test principles, Design for testability (DFT) -

Adhoc testing, Scan design, Built in self-test (BIST)
Xilinx3000Series, Boundary scan

Practical components

1. Design and ASIC Implementation of 4:1 MUX
2. Design and FPGA Implementation of 2:4 Decoder
3. Design and FPGA Implementation of a D-Latch
4. Perform the ASIC implementation of a 4-bit counter

12+8 Hours
Total: 48+32 Hours

Textbooks:

1. Kamran Eshraghian, Douglas ,A. Pucknell And Sholeh Eshraghian, Essentials of VLSI Circuits and Systems, , Prentice-Hall of India Private Limited, 2005 Edition.
2. Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill, 2003
3. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, Digital Integrated Circuits, Pearson Education, 2nd edition,2016.
4. Weste and Eshraghian, Principles of CMOS VLSI Design, Pearson Education, 3rdEdition, 1999
5. Michael john Sebastian smith, Application specification integrated circuits, Addition Wesley,1st edition,1997

References:

1. John P. Uyemura, ,Introduction to VLSI Circuits and Systems, John Wiley & Sons, reprint 2009.
2. Vinod Kumar Khanna, Integrated Nanoelectronics: Nanoscale CMOS, Post-CMOS and Allied Nanotechnologies, Springer India, 1st edition, 2016.
3. Michael John Sebastian Smith, Application Specific Integrated Circuits, Addison-Wesley, 1997.

SAMPLE QUESTION (S)
Internal Assessment Pattern

Cognitive Level	Int Test 1 (%)	Int Test 2 (%)	Lab Examination(%)
Remember	35	20	--
Understand	40	30	--
Apply	25	50	100
Analyze	--	--	
Evaluate	--	--	--
Create	--	--	--
Total %	100	100	100

Remember

1. What are the scaling models?
2. Why switch logic is better than pass transistor logic?
3. Show that pull up to pull down ratio of an nMOS inverter driven by another nMOS inverter is
4. How the delay varies with number of inputs for different fabrication processes?
5. Show that 11 is the best test vector for AND gate if there is a SA0 fault on one node

Understand

1. Explain briefly about nMOS pass transistor
2. Compare Stick diagram and Layout
3. Explain about λ based design rules in detail
4. Classify possible wiring capacitances in VLSI fabrication process
5. Explain about architecture of FPGA.

Apply

1.Construct CMOS inverter having pull up to pull down ratio of 1:1 if n channel sheet resistance is 10kΩ and p channel sheet resistance is 25kΩ
2. Construct layout for 2-input NAND gate

3. Show the architecture of FPGA with neat sketch
4. Demonstrate your answer , If the disturbance is created at the output then there exist low resistance path between supply rails of CMOS inverter, is that disturbance creates problem in the CMOS inverter,
5. Construct Enhancement load and depletion load nMOS inverters

21EC504 Antennas and Microwave Engineering

3 0 0 3

Course Outcomes

1. Illustrate parameters of an antenna and antenna arrays
2. Implement antenna arrays
3. Design an antenna for given specifications
4. Justify modes of rectangular waveguide and the S-parameters of waveguide components
5. Summarize operation of microwave tubes
6. Interpret microwave measurements

COs – POs Mapping

COs	PO_1	PO_2	PSO_2
1	2	-	2
2	3	2	3
3	3	2	3
4	3	2	3
5	2	-	2
6	2	-	2

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Antenna Fundamentals & Uniform Linear Arrays

Radiation Mechanism: Single wire, Two wire, Dipoles, Current Distribution on a thin wire antenna, Antenna Parameters: Radiation Patterns, Patterns in Principal Planes, Main Lobe and Side Lobes, Beam width, Beam Area, Bandwidth, input impedance, Radiation Intensity, Beam Efficiency, Directivity, Gain, Antenna Apertures, Antenna efficiency, Antenna regions, Friis Transmission equation.

Antenna arrays: Different cases of 2 element arrays, Principle of Pattern Multiplication, N element Uniform Linear Arrays: Broadside and End fire Arrays. Introduction to LiDar.

Binomial array and it's applications **13 Hours**

Unit II

Arrays with Parasitic Elements and Special Antennas

Arrays with Parasitic Elements: Yagi Uda Arrays, Folded Dipoles & their characteristics, Paraboloidal Reflectors: Geometry, characteristics, types of feeds, F/D Ratio, Spill Over, Back Lobes, Aperture Blocking, Off-set Feeds and Cassegrain Feeds.

Helical Antennas: Significance, Geometry, basic properties, Design considerations for monofilar helical antennas in Axial Mode and Normal Modes (Qualitative Treatment), Horn Antennas - Types, Optimum Horns, Design Characteristics of Pyramidal Horns, Design of Rectangular and Circular Microstrip Patch antenna, Log Periodic antennas - Introduction, Planar wire surfaces.

Applications of microstrip patch antenna and Lens antennas **11 Hours**

Unit III

Waveguides and Wave Guide Components

Introduction: Microwave Spectrum, advantages and applications of microwaves, Rectangular waveguides- TE/TM mode analysis, Expressions for Fields, Characteristic Equation and Cut-off Frequencies, Dominant and Degenerate Modes, Mode Characteristics: Phase and Group Velocities.

Scattering Matrix: Significance, Properties, S Matrix Calculations for multi-port Junctions - E plane and H plane Tees, Magic Tee, Directional Coupler, Faraday rotation devices- Gyrator, Isolator, Circulator.

Hybrid Rings and rat race junction

14 Hours

Unit IV

Microwave Tubes and Microwave Measurements

Limitations and Losses of conventional tubes at microwave frequencies, Two Cavity Klystron - Velocity Modulation and Applegate Diagram, Bunching Process. Reflex Klystron - Applegate Diagram and Principle of working, Magnetron - 8-Cavity Cylindrical Travelling Wave Magnetron.

Microwave Bench- Different Blocks and their Features, Precautions, Microwave Power Measurement: Bolometer Method, Measurement of Attenuation, Frequency, VSWR, Impedance Measurement.

Applications Gunn Diode and Impatt diode

10 Hours

Total: 48 Hour

Textbook (s)

1. C.A Balanis, Antenna Theory, John Wiley & Sons, 3rd Edition. 2016
2. John D Krauss, Ronald J Marhefka, Ahmad S Khan, Antennas for all applications, Tata McGraw-Hill, 3rd Edition, 2009
3. K. D. Prasad, Antennas & Wave Propagation, Satya Prakashan, New Delhi, 3rd Edition, 2011
4. Samuel Y. Liao, Microwave Devices and Circuits, Pearson education, 3rd Edition, 2007
5. Pozar, Microwave Engineering, Wiley publishers, 4th Edition, 2012

Reference (s)

1. E.C. Jordan and K.G. Balmain, Electromagnetic Waves and Radiating Systems, PHI, 2nd Edition, 2011
2. John D Kraus, Antennas, Tata McGraw-Hill, 2nd Edition, 2001
3. R.E. Collin, Foundations for Microwave Engineering, IEEE Press, John Wiley, 2nd Edition, 2000
4. M. Kulkarni, Microwave and Radar Engineering , Umesh Publications, 4 th Edition, 2010

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	40	40	--
Understand	30	30	--
Apply	30	30	60
Analyse	--		40
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. Define directivity and gain of an antenna.
2. List out the different antennas under use
3. State any two differences between broad side array and end fire array
4. Define dominant mode
5. Define degenerate mode

Understand

1. Explain directivity in terms of radiation intensity and power density.
2. Explain radiation mechanism of two wire.
3. Compare TE and TM modes of a wave guide.
4. Identify the conditions of occurrence of degenerating modes.
5. Compare the E-plane Tee and H-plane Tee in any four aspects.

Apply

1. Design a rectangular patch antenna which should be operated at a frequency of 10 GHz with a radius of 3 inchs for an FR4 substrate material.
2. Show that TE10 mode is the dominant mode in rectangular waveguide.

[Open Book Examination Questions]
Apply

1. The input power in a two hole directional coupler is 1mW. The coupler has a coupling factor of 15 dB and a directivity of 30 dB. Compute the power in all the ports.
2. Design a uniform linear broadside antenna array of N elements placed along the z- axis with a uniform spacing d=1/10 between the elements. Determine the closest integer number of elements so thst in the elevation plane:
   (a) the half-power beam width of the array factor is approximately 60^0
   (b) the first-null beam width of the array factor is 60^0

Analyse

1. Justify that it is impossible to construct a perfectly matched, lossless, reciprocal three port junction.
2. Two lossless X-band (8.2–12.4 GHz) horn antennas are separated by a distance of 100λ. The reflection coefficients at the terminals of the transmitting and receiving antennas are 0.1 and 0.2, respectively. The maximum directivities of the transmitting and receiving antennas (over isotropic) are 16 dB and 20 dB, respectively. Assuming that the input power in the lossless transmission line connected to the transmitting antenna is 2W, and the antennas are aligned for maximum radiation between them and are polarization-matched, find the power delivered to the load of the receiver.

21ECC11 RTL Coding Techniques

3 0 0 3

Course Outcomes:

1. Interpret the RTL design guidelines and synthesis of procedural blocks
2. Illustrate the Verilog RTL coding techniques
3. Use the RTL design techniques in HDL coding of digital circuits
4. Demonstrate the RTL design techniques for the implementation of sequential and combinational blocks
5. Perform the RTL coding at block level for a digital system architecture
6. Interpret the control path and data path for complex digital circuits

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PSO_1
1	2	-	-	2
2	2	-	-	2
3	3	2	2	3
4	3	2	2	3
5	3	2	2	3
6	3	2	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

RTL Coding Techniques-I

Introduction to Verilog & Modelling Styles, RTL Design Guidelines, Parallel Versus Priority Logic, Blocking Assignments and Event Queue, Blocking Assignments and multiple "always" blocks, Blocking Assignments in the same "always" block, ordering of non-blocking assignments, Continuous versus Procedural Assignments, Combinational Loops in Design.

RTL code for Subtraction using 2's complement, ALU

12 Hours

Unit II

RTL Coding Techniques-II

Sequential statements - 'case' with missing 'default', 'if-else' with missing 'else', Logical Equality versus Case Equality, Incomplete Sensitivity List, Unintentional Latches in the Design, if-else versus case statements, Arithmetic Resource Sharing, Asynchronous Reset D flip-flop, Synchronous Reset D flip-flops, Gated Clocks, Clock Enables

RTL code for 2 to 4 decoder using conditional statement, Synthesize the RTL for 4 to 1 Mux missing else

12 Hours

Unit III

RTL Coding Practice

State Machines and Optimization, Moore Machine, Mealy Machine, Sequence Detectors using FSM's, Design without Pipelining, Design with Pipelining, Synchronous Counters: Up-Down Counter, Ring Counter, Johnson Counter, Asynchronous Counter: Ripple Counter; Structured design of nibble adder, Multiplexer, Decoder

RTL code for the encoder, decoder, shift registers

12 Hours

Unit IV

RTL Coding for Digital Architectures

Tri-State Bus, Bus Arbitration, Static Arbitration, Bidirectional Data Transfer, RTL design for**,** Single-Port RAM, Dual-Port RAM**,** RTL design for Serial adder: Control path and Data path

SDRAM Memory Controller, DDR Memory Controller

12 Hours

Total: 48 Hours

Textbook (s)

1. Vaibbhav Taraate, Advanced HDL Synthesis and SOC Prototyping (RTL Design Using Verilog), Springer Nature Singapore Pte Ltd., 2019
2. Vaibbhav Taraate, Digital Logic Design Using Verilog Coding and RTL Synthesis, Springer Nature Singapore Pte Ltd., 2016
1. J Bhasker, A Verilog HDL Primer, Star Galaxy Publishing, 3rd Edition, 2018

Reference (s)

1. Michael D. Ciletti, Advanced Digital Design with the Verilog, Prentice-Hall of India Private limited, 2nd Edition, 2005

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	20	20	--
Understand	55	40	--
Apply	25	40	60
Analyse	--	--	40
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. Define Verilog module structure
2. List out any two sequential statements with syntax
3. List out any four Verilog operators
4. List out any three modelling styles of Verilog HDL
5. State the procedural constructs in Verilog
6. Define static arbitration

Understand

1. Illustrate the concept of case statement
2. Interpret the concept of if – else statement
3. Compare Moore and Mealy machines
4. Explain the concept of Arithmetic Resource Sharing an example
5. Explain Gated Clocks with suitable example
6. Compare asynchronous reset and synchronous reset D flip-flops

Apply

1. Construct Verilog HDL for 4 to 1 multiplexer
2. Design 4-bit parallel adder using full adders
3. Design 2-input OR gate using multiplexer
4. Construct Verilog HDL for one bit comparator
5. Construct the RTL design to implement FIFO memory buffer
6. Construct the RTL design to implement digital circuit (with minimum gates and flip flops) that could control a coin operated vending machine to dispenses a candy under following conditions:
   (a) The machine accepts only Rs. 5 coin and other than Rs. 5 coin it should not accept.
   (b) It takes Rs. 15 for a piece of candy to be released from the machine
      i. Develop a state table and state diagram.
      ii. Draw the architecture in terms of control path and data path.
      iii. Construct the RTL to implement the above architecture.

[Open Book Examination Question]

Analyze

1. Compare blocking and non-blocking assignments
2. Differentiate continuous assignment and procedural assignment statements with an example
3. Resolve the concept of with and without pipelining
4. Compare the gate level implementation of D flip-flop
5. Compare initial and always constructs in Verilog HDL
6. Integrate a simplified traffic-light controller that switches traffic lights on a crossing where a north-south (NS) street intersects an east-west (EW) street. The input to the controller is the WALK button pushed by pedestrians who want to cross the street. The outputs are two signals NS and EW that control the traffic lights in NS and EW directions. When NS or EW is 0, the red light is on and when they are 1, the green light is on. When there are no pedestrians, NS=0 and EW=1 for 1

minute, followed by NS=1 and EW=0 for 1 minute and so on. When a WALK button is pushed, NS and EW both come 1 for a minute when the present minute expires. After that the NS and EW signals continue alternating. For the traffic-light controller:

i. Develop a state table and state diagram.
ii. Draw the architecture in terms of control path and data path
iii. Construct the RTL to implement the above architecture

[Open Book Examination Question]

21ECC21 Data Acquisition System

3 0 0 3

Course Outcomes

1. Illustrate various digital data acquisition systems
2. Assess various data transfer techniques
3. Demonstrate the working principle of serial interface
4. Demonstrate the working principle of various digital instruments
5. Interpret various signal condition techniques
6. Outline various Remote data Acquisition techniques

COs – POs Mapping

COs	PO_1	PO_2	PSO_1
1	2	-	2
2	3	2	3
3	3	2	3
4	3	2	3
5	2	-	2
6	3	3	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Data Acquisition systems & control

Use of signal conditioners, scanners, signal converters, recorders, display devices, A/D & D/A circuits in digital data acquisition, Instrumentation systems: Types of Instrumentation systems, Components of an analog Instrumentation Data – Acquisition system. Multiplexing systems, Uses of Data Acquisition Systems, Use of Recorders in Digital systems, Digital Recording systems, Modern Digital Data acquisition system, Analog Multiplexed operation, operation of sample Hold circuits.

sample & hold circuits- specifications and design considerations.

12 Hours

Unit II

Data Transfer Techniques:

Interfacing To PC: Expansion Buses- ISA Bus, EISA Bus, PCI Bus. Plug in data Acquisition and Control Boards: Functions of Plug in DAQ boards, Design of General purpose DAQ boards, Design of DAQ boards for PCI Bus. Data Acquisition using Serial Interface: Serial Interface Standards Rs 232, USB-Features of USB, USB system, USB Transfer, USB Descriptors, GPIB/IEEE-488, LAN, Universal serial bus, HART protocol, Zigbee and Bluetooth.

Foundation Field bus, ModBus

12 Hours

Unit III

Digital Instruments

Digital voltmeters (DVMs): working principle, construction, operation, salient features, range selection– Ramp type, dual slope integrating type, successive approximation type, Digital Frequency Meter: working principle, construction (block diagram), range selection and operation of, time period meter, frequency ratio meter, Recorders: The working principle, construction, operation and salient features of X-t strip chart recorder, Introduction to PLC

X-Y strip chart recorder and Magnetic type recorder. **12 Hours**

Unit IV

Signal Conditioning and DAQ Systems

Single channel and multichannel, Graphical Interface (GUI) Software for DAS, RTUs, PC-Based data acquisition system , Data logging - applications - Automobile, Aerospace Manufacturing, Environmental monitoring. Temperature Measurement using Thermistor, Thermocouple, Strain Measurement System, Interfacing Piezo electric Actuator and sensor, Interfacing Light Emitting Diode and Photo sensor, Acceleration Measurement, Function Generator, DC position servomotor control, Remote data Acquisition using Internet, Machine vision-based inspection system. IC engine data

12 Hours

Total: 48 Hours

Text Books

1. Di Paolo Emilio, Maurizio , “Data Acquisition Systems From Fundamentals to Applied Design”,

Springer; 2013.
2. S. Gupta, J.P. Gupta, PC Interfacing for Data Acquisition and Process Control, ISA, 1994, 2nd Edition
3. Bell David A, "Electronic Instrumentation and Measurement", PHI, Inc, New Delhi (1994).
4. Tocci Ronald J , "Digital Systems Principles and Applications", PHI, New Delhi (2002)

Reference Books

1. A. D. Helfrick and W.D. Cooper, "Modern Electronic Instrumentation and Measuring Techniques", Pearson, 1st Edition, 2015.
2. R. K. Jain , "Mechanical & Industrial Measurements", Khanna pub.
3. Chennakesava R Alavala, "Principles of Industrial Instrumentation and control systems", Cengage publ.

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open book Examination (%)
Remember	25		--
Understand	35	25	--
Apply	20	45	60
Analyse	20	30	40
Evaluate	--		--
Create	--		--
Total (%)	100	100	100

Remember

1. List the Converter Characteristics and explain them
2. Discuss the objectives of DAS.
3. Explain the following terms in detail (i) Resolution (ii)Non-linearity (iii)settling time (iv) Monotonicity

Understand

1. Draw the circuit diagram of Polynomial converter and explain its operation in detail
2. Explain the concept of Digital signal processing system in Digital Acquisition System along with circuit diagram
3. Define Error? Explain the different Error sources present in ADC and DAC systems in detail

Apply

1. Design a digital Voltmeter of range 0 to 20 v
2. Determine the working principal of HART protocol
3. Construct a digital frequency meter
4. Analyze various data loggers
5. Justify the working principal of Machine vision-based inspection system. IC engine data
6. Compare Various Remote data Acquisition using Internet

[Open Book Examination Question]

21ECC31 Information Theory and Coding Techniques

3 0 0 3

Course Outcomes

1. Exemplify the information theory concepts and channel capacity
2. Explain various kinds of channels and Shannon theorem
3. Outline various source coding techniques
4. Demonstrate the generation and detection of error control codes
5. Summarize the channel coding techniques
6. Outline the encoding and decoding structure of convolutional codes

COs-POs Mapping

COs	PO_1	PO_2	PSO_2
1	2	1	2
2	2	1	2
3	3	2	3
4	3	2	3
5	2	1	2
6	3	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I
Information Theory

Concept of information, Mutual information, Entropy: marginal, conditional, joint and relative entropies, relation among entropies, Mutual information, information rate, channel capacity, redundancy and efficiency of channels, Discrete channels: Symmetric channels, Binary Symmetric Channel, Binary Erasure Channel, Noise-Free Channel, Shannon's theorem.

Differential entropy, Gaussian channel

12 Hours

Unit II
Source coding

Introduction to source coding, purpose of encoding, Instantaneous codes, construction of instantaneous codes, Kraft's inequality, coding efficiency and redundancy, source coding theorem. construction of basic source codes, Shannon Fano coding, Huffman coding, Channel coding theorem for DMC (Discrete memoryless channel).

Rate-distortion function, Quantization

12 Hours

Unit III
Error Control Coding

Codes for error detection and correction: Parity check coding, Linear block codes, Error detecting and correcting capabilities, Generator and Parity check matrices, Standard array and Syndrome decoding, Hamming codes, Cyclic codes: Generator polynomial, Generator and Parity check matrices, Encoding of cyclic codes, Syndrome computation and error detection, Decoding of cyclic codes.

BCH Code, Golay code

12 Hours

Unit IV
Convolutional Codes

Encoding and state, Tree and Trellis diagrams, Maximum likelihood decoding of convolutional codes, Viterbi algorithm, Sequential decoding. Automatic repeat request(ARQ), Performance of ARQ, Probability of error and throughput, Applications: Concatenated Codes, Interleavers, The Compact Disc, Codes for Magnetic recording.

RS code, Turbo code

12 Hours
Total: 48 Hours

Textbook (s)

1. Stephen.B.Wicker, Error Control Systems for Digital Communication and storage, Prentice Hall,1995.
2. Bernard Sklar, Digital communications: Fundamentals and applications, 2nd Edition, Prentice Hall,2001.
3. Simon Haykin, Communication Systems, 4th Edition, John Wiley and Sons, 2001.

Reference (s)

1. John G.Proakis, Digital communication, 4th edition, McGraw Hill, 2001.
2. R.P. Singh, SP Sapre, Communication Systems, 3rd Edition, TMH, 2017.

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	25	20	--
Understand	50	40	--
Apply	25	25	80
Analyse	--	15	20
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. Define mutual information
2. State Shannon Hartely theorem
3. List any two block codes
4. List any two source code techniques
5. Define maximum likelihood probability
6. List any two applications of convolutional codes

Understand

1. Explain various types of error channels.
2. Illustrate the structure of Shannon fano coding.
3. Compare Shannon fano and Huffman coding.
4. Illustrate the detection of cyclic codes.
5. Represent the Viterbi decoding algorithm and explain the steps in decoding.
6. Explain the applications of convolutional codes.

Apply

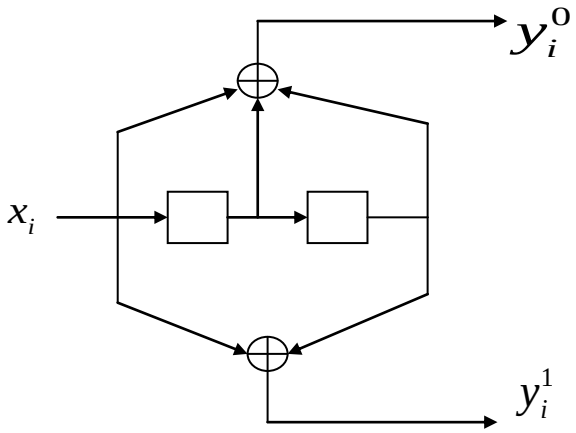
1. A source emits a sequence of symbols having probabilities given below.
   {0.4, 0.2, 0.12, 0.08, 0.08, 0.08, 0.04}.
   a) Using Shannon-fano algorithm find out the average code word length, entropy and efficiency of the source for single-partitioning.
   b) Determine the same by performing Huffman-coding algorithm
2. Consider a (7, 4) Code whose Generator matrix is given below.
   a) Find all the codewords of the code. What is $d_{\min}$?
3. A discrete memoryless source has an alphabet of seven symbols having probabilities of occurrence as {0.25,0.25,0.125,0.125,0.125,0.0625,0.0625}.Compute the Huffman code for this source, moving a "combined" symbol as high as possible. Show that the efficiency of source code is 100 percent.
   [Open Book Examination Question]
4. Design a feedback shift register encoder for an (8, 5) cyclic code with a generator. Use the encoder to find the codeword for the message 10101 in systematic form.
   [Open Book Examination Question]

Analyse

1. For the convolutional encoder shown below, determine the following:

a) Output sequence for message sequence x_i ={1 0 0 1 1} in both time domain and transform domain approach.
b) Construct the state diagram for corresponding encoder.

2. Prove the Statement "The mutual information of a channel is related to the joint entropy of the channel input and channel output"
3. a) The generator polynomial of a (15,11) hamming code is defined by g(X) =1+X+X^4 develop the encoder and syndrome calculator for the code.
   b) Encode the 1 0 1 in systematic form using polynomial division and the generator g(X) = 1+X+X^2+X^4.
   [Open Book Examination Question]
4. For the convolutional encoder shown below, determine the following:
   a) Output sequence for message sequence x_i ={1 0 1 0 1} in both time domain and transform domain approach.
   b) Draw the state diagram for corresponding encoder.



[Open book Examination Question]

21IT304 Database Management Systems

3 0 0 3

Course Outcomes

1. Understand the fundamental concepts of data base and data models
2. Explain the use of Relational Algebra and integrity constraints in databases
3. Use SQL's Commands to handle the Database
4. Apply Normalization for schema refinement
5. Make use of the concept of transaction management and recovery system in databases
6. Outline Indexing concepts, different types of data

CO–PO Mapping

COs	PO_1	PO_2	PO_3
1	3	3	2
2	3	3	3
3	3	3	2
4	2	3	3
5	3	3	3
6	3	3	2

3–Strongly linked | 2–Moderately linked | 1–Weakly linked

Unit I

Introduction to DBMS and ER Model

DBMS Vs. File System, instance and schema, Data abstraction, Data independence, database users and database administrator, Database system structure, Introduction to Data Models (E-R Model, Relational Model, Hierarchical Model, Network Model, Object Oriented Data Model), Database Design Process, Entities, Attributes, Entity Sets, Relationships, Relationship Sets, Additional features of ER Model.

Applications of DBMS, Object Relational Data Model **12Hours**

Unit II

Introduction to Relational Model and Basic SQL Queries

Relational Algebra Operations: Selection, Projection, Rename, Set Operators, Joins, Division, Examples of Relational Algebra Queries, Relational Calculus: Tuple Relational Calculus.

Integrity Constraints over Relations, Introduction to Views.

SQL Queries: Basic Structure, Set Operations, Aggregate Functions, Null values, Sub Queries, Group By And Having Clauses, Outer Joins.

Domain Relational Calculus, Query Optimization **12Hours**

Unit III

Normalization and Transaction Management

Introduction To Schema Refinement - Problems Caused By Redundancy - Decomposition - Problems Related To Decomposition - Functional Dependency - Closure of a Set of Fds - Attribute Closure - First - Second - Third Normal Forms – BCNF - Multi Valued Dependencies – Fourth Normal Form, Join Dependency, Fifth Normal Form

Transactions: Acid Properties of Transaction - Transaction States - Schedule: Serial Schedule - Concurrent Schedules - Anomalies Associated with Concurrent Schedules (RW - WR - and WW Conflicts) -Serializability - Conflict Serializability - and View Serializability.

EF Codd Rules, Domain Dependency **12 Hours**

Unit IV

Locking, Recovery Systems, Indexing, Different Types of Data

Introduction to Lock Management-Lock Based Concurrency Control: 2pl-Strict 2pl-Concurrency without Locking: Timestamp–Based Concurrency Control, Optimistic Concurrency Control.

Introduction to Aries - the Log - the Write-Ahead Log Protocol-Check Pointing Indexing: Types of Single-Level Ordered Indexes, Multilevel Indexes Different Types of Data: Structured, Semi-Structured and Unstructured Data

Heap File, Hash File Organizations **12 Hours**

Total: 48 Hours

Textbook (s)

1. Elmasri & Navatha, Fundamentals of Database Systems, Pearson Education, 7th Edition, 2016

2. Silberschatz Korth, Database System Concepts, McGraw hill, 7th Edition, 2019

Reference (s)

1. Soraya Sedkaoui, Data Analytics and Big Data, Wiley, 1st Edition, 2018.
2. Peter Rob & Carlos Coronel, Database Systems design, Implementation and Management, 9th Edition, 2010.
3. Raghurama Krishnan & Johannes Gehrke, Database Management Systems, TATA McGraw-Hill, 3rd Edition, 2003
4. C.J.Date, An Introduction to Database Systems, Pearson Education, 8th Edition, 2006

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	40	40	--
Understand	30	40	--
Apply	30	20	50
Analyze	--	--	50
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Sample Question (S)

Remember

1. List any four application of DBMS
2. Define data model
3. List any four applications for triggers
4. Define functional dependency
5. List the 4 properties of Transaction

Understand

1. Explain E-R Model with suitable example
2. Explain the role of integrity constraints in database design
3. Illustrate the working principle of 'write a head log' protocol
4. Differentiate 3NF and 4NF
5. Explain Two Phase Locking Protocol

Apply

1. When multiple transactions are being executed by the operating system in a multiprogramming environment, there are possibilities that instructions of one transaction are interleaved with some other transaction. Apply the suitable concept to overcome the problem
2. Classify various normal forms according to their applicability
3. Give some real-world applications of Normalization
4. Illustrate the Commit and Rollback operations of Transaction Control
5. Give some real-world applications for Database indexing techniques

Analyze

1. Compare File processing system with DBMS
2. Analyze different locking protocol for concurrency control and serializability
3. Normalization will increase the complexity of the database design. Justify
4. Compare DDL and DML of SQL
5. Compare and Contrast Serializability and Recoverability

Evaluate

1. Is database redesign being necessary? explain
2. How can you evaluate the performance of two data models?
3. Evaluate the performance of query processor and list the corresponding metrics
4. How can you assess the throughput and delay for any DBMS?
5. How can you evaluate the impact of data models on the query processing?

Open Book Examination Questions

1. Anitha has a large CD collection. Her friends like to borrow her CD's, and she has to keep track of who has what. She maintains a list of friends, identified by unique FID's and a list of CD's, identified

by CID's. With each friend are the name and telephone numbers which she can call to get the CD back. With each CD is actor name and title. Whenever a friend borrows a CD, She will enter that fact into her database along with the date borrowed. Whenever the CD gets returned, that fact, too, gets noted along with the date returned. Anitha wants to keep a complete history of her friends' borrowing habits so that she can ask favors of the heavy borrowers.
Draw an ER diagram to figure out the above situation and identify types of attributes and cardinality. Represent this database as a collection of 3NF relational tables.

2. The relational scheme R(A,B,C,D,E,F) and set of functional dependencies AB -> D, E -> C, AF -> B. From this, find out all super keys for this relation, and which of these super keys form a key.

21CS303 Data Structures

3 0 0 3

Course Outcomes

1. Describe the operations and implementation of List ADT
2. Comprehend the operations and implementation of Stack and Queue
3. Illustrate the applications of linear data structures
4. Describe the operations and implementation of hash table
5. Comprehend the operations and implementation of tree data structure
6. Illustrate the variations of tree data structure

CO-PO Mapping

CO	PO1	PO2
1	3	2
2	3	2
3	2	3
4	2	3
5	3	2
6	2	3

3–Strongly linked | 2–Moderately linked | 1–Weakly linked

Unit I

Linear Data Structures – List

Abstract Data Types (ADTs) – List ADT – Array-based implementation – Linked list implementation –Singly linked lists- Circularly linked lists- Doubly-linked lists – Applications of lists –Polynomial Manipulation – All operations (Insertion, Deletion, Merge, Traversal) - Searching - Linear Search – Binary Search

Doubly linked Circular list **12 Hours**

Unit II

Linear Data Structures – Stack and Queue

Stack ADT – Array implementation – Linked list implementation – Applications of Stack – infix to postfix conversion, evaluation of postfix expression – Queue ADT – Array implementation – Linked list implementation – Application of Queue – Ticket counter

Circular Queue **12 Hours**

Unit III

Sorting, Hashing Techniques and Trees

Sorting – Bubble Sort – Selection Sort – Insertion Sort – Shell Sort – Radix Sort – Quick Sort – Merge Sort - Hashing - Hash Functions – Separate Chaining – Open Addressing – Rehashing

Trees: Introduction, Terminology, Binary Trees, Representation of Binary Trees using arrays and linked lists, Binary tree traversals

Extendible Hashing **12 Hours**

Unit IV

Variations on Trees and Graphs

Binary Search Trees: definition, basic operations of BST (Searching, Insertion and deletion) - Introduction to AVL trees: Balancing AVL tree by rotations after insertions and deletions of a data node Multi-way search trees: Introduction to m-way search trees, B-trees, B+ Trees;

Heaps: Binary heaps, definition of a Max-heap, Min-heap, Creating Max-Heap, Applications: Heap sort

Graphs: Terminology, Representation, Traversals: Depth First Search and Breadth First Search

Priority queue operations: insertions and extract-max

12 Hours

Total: 48 Hours

Textbook (s)

1. Mark Allen Weiss, Data Structures and Algorithm Analysis in C, Pearson Education, 2002
2. Michael Main, Walter Savitch, Data Structures and other objects using C++, 4th Edition, Addison Wesley, 2018

Reference (s)

1. S. Tanenbaum, Y. Langsam and M.J. Augenstein,, Data Structures using C and C++, 2nd Edition, Pearson Education, 2015

2. R. F. Gilberg, B. A. Forouzan, Data Structures A Pseudocode Approach with C, 2nd Edition, CENGAGE Learning, 2005

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Examination (%)
Remember	20	20	--
Understand	60	60	--
Apply	20	20	80
Analyze	--	--	20
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

SAMPLE QUESTION (S)

Remember

1. What are abstract data types?
2. List any 2 disadvantages of array
3. Define linked list
4. Define data structure
5. List any 2 applications of queue

Understand

1. Compare linked list with array
2. Explain Bubble Sort Process with an example
3. Demonstrate with neat diagram and algorithm to insert a node before the given key
4. Explain Deletion process using an example binary search tree
5. Explain why the selection sort is more efficient than the bubble sort
6. Explain with suitable example of LL rotation after inserting a new node into an AVL tree
7. Demonstrate the application of singly linked lists for the addition of the polynomials P1 and P2

Apply

1. Develop an algorithm to concatenate two single linked lists
2. Construct a priority queue and implement all basic operations to demonstrate priority queue
3. Build a recursive procedure to count the number of nodes in a binary tree

Sample Questions for Open Book Examination

Apply

1. Select appropriate data structure to simulate the operations of a Music Player – Songs in music player are linked to previous and next song. you can play songs either from starting or ending of the list.

2. A bracket is considered to be any one of the following characters: (,), {, }, [, or]. Two brackets are considered to be a matched pair if the an opening bracket (i.e., (, [, or {) occurs to the left of a closing bracket (i.e.,),], or }) of the exact same type. There are three types of matched pairs of brackets: [], {},and (). A matching pair of brackets is not balanced if the set of brackets it encloses are not matched. For example, {[(])} is not balanced because the contents in between { and } are not balanced. The pair of square brackets encloses a single, unbalanced opening bracket, (, and the pair of parentheses encloses a single, unbalanced closing square bracket,].

By this logic, we say a sequence of brackets is balanced if the following conditions are met: It contains no unmatched brackets. The subset of brackets enclosed within the confines of a matched pair of brackets is also a matched pair of brackets. Given n strings of brackets, determine whether each sequence of brackets is balanced. If a string is balanced, return YES. Otherwise, return NO.

3. You are given a stack of **N** integers such that the first element represents the top of the stack and the last element represents the bottom of the stack. You need to pop at least one element from the stack. At any one moment, you can convert stack into a queue. The bottom of the stack represents the front of the queue. You cannot convert the queue back into a stack. Your task is to remove exactly **K** elements such that the sum of the **K** removed elements is maximized.
4. Vikas is given a bag which consists of numbers (integers) blocks, Vikas has to organize the numbers again in the same order as he has inserted it into the bag, i.e. the first number inserted into the bag by Vikas should be picked up first followed by other numbers in series. Help Vikas to complete this work in O(n) time complexity with the condition to use one extra bag to complete the work (assume that the bags are compact and is in the form of a stack structure and has the same width as that of the number blocks and is large enough to fill the bag to the top and the number taken from bag is in reverse order).

21CS403 Computer Organization and Architecture

3 0 0 3

Course Outcomes

1. Interpret the functional architecture of computing systems. (Understand).
2. Summarize the types of instruction and its micro operation with addressing modes (Understand)
3. Identify various arithmetic operations on fixed, floating point numbers and its representation (Apply)
4. Illustrate the concepts of control unit design and I/O processor(Understand)
5. Understand the memory hierarchy concepts (Understand)
6. Describe concept of parallelism and types of hazard(Understand)

CO-PO Mapping

CO	PO1	PO2
1	3	2
2	2	-
3	3	1
4	3	2
5	3	2
6	2	-

3–Strongly linked | 2–Moderately linked | 1–Weakly linked

Unit I

Overview & Microoperation

Components of a computer system – Performance measures - Classifying Instruction Set Architecture-Representing instructions -Micro operation – Logical operations – Shift operations - instruction codes - Computer Registers instruction –memory Reference instruction –Input-Output Reference instruction - Instruction cycle -Addressing and addressing modes.

Trends in Technology-Arithmetic micro-operations **13 Hours**

Unit II

Arithmetic Operations

ALU - Addition and subtraction with Signed Magnitude Data - Hardware Implementation – Multiplication – Hardware Implementation for Signed Magnitude Data – Division - Hardware Implementation for Signed Magnitude Data – Divide Overflow - Floating Point operations – Parallelism and Computer Arithmetic: Sub word Parallelism.

BCD Adder-BCD Subtraction **11 Hours**

UNIT III

Control Unit and Memory Systems

Basic MIPS implementation – Building data path – Control Implementation scheme – Memory hierarchy – Cache basics – Measuring and improving cache performance - Virtual memory- Input/output system-programmed I/O-DMA and Interrupts-I/O processors

Stack organization-RISC Vs CISC Architecture **13 Hours**

Unit IV

Parallelism

Instruction-level-parallelism – Parallel processing challenges – Flynn's classification – Multicore processors-Pipelining – Arithmetic pipeline –Instruction pipeline -Pipelined data path and control – Handling Data hazards & Control hazards – Exceptions.

Vector processing –single processor Vs parallel processor **11 Hours**

Total: 48 Hours

Text Book(s):

1. David A. Patterson and John L. Hennessey, "Computer organization and design: The hardware /software interface", Morgan Kauffman / Elsevier, Fifth edition, 2014
2. M.Morris Mano," Computer System Architecture", 3rd edition, Pearson /PHI,1992.

Reference(s):

1. V.Carl Hamacher, Zvonko G. Varanesic and Safat G. Zaky, "Computer Organization ", 6th edition, Mc Graw-Hill Inc, 2012.
2. William Stallings "Computer Organization and Architecture, Seventh Edition, Pearson Education, 2007.
3. Andrew S Tanenbaum "Structured Computer Organization ", 5th edition, Pearson/PHI, 2007

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open book Exam (%)
Remember	40	--	--
Understand	40	50	--
Apply	20	50	80
Analyze	--	--	20
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

SAMPLE QUESTION (S)

Remember

1. What is micro operation?
2. Show the Register Reference Instruction format.
3. Define PC and MAR.
4. What are the two types of data representation?
5. Define Associative Memory

Understand

1. Identify the basic functional units of the system
2. Explain about logic micro operations and its applications with examples
3. Differentiate RISC and CISC architecture in terms of their instruction set and addressing modes.
4. Compare hardwired control unit is differing from micro programmed control unit designs
5. Demonstrate control memory

Apply

1. Starting from an initial value of R=11011101, determine the sequence of binary values in R after a logical shift-left, followed by a logical shift-right and a circular shift-right.
2. Analyze the contents of Register A that holds 8 bit binary 11011001 and Determine the B-operand and the logic micro operation to be performed in order to change the value in A to: (i) 01101101 (ii) 11111101State the differences between register stack and memory stack.
3. Perform the arithmetic operations (+70) + (+80) and (-70) + (-80) with binary numbers in signed-2's complement representation. Use eight bits to accommodate each number together with its sign. Show that overflow occurs in both cases, that the last two carries are unequal, and that there is a sign reversal.
4. Show the hardware to be used for the addition and subtraction of two decimal numbers with negative numbers in signed- 10's complement representation. Indicate how an overflow is detected. Derive the flowchart algorithm and try a few numbers to convince yourself that the algorithm produces correct results.
5. The procedure for aligning mantissas during addition or subtraction of floating-point numbers can be stated as follows: Subtract the smaller exponent from the larger and shift right the mantissa having the smaller exponent a number of places equal to the difference between the exponents. The exponent of the sum (or difference) is equal to the larger exponents. Without using a magnitude comparator, assuming biased exponents, and taking into account that only the AC can be shifted, derive an algorithm in flowchart form for aligning the mantissas and placing the larger exponent in the AC **[Open book questions]**

Apply

1. Smith and Goodman found that for a given small size, a direct –mapped instruction cache consistently outperformed a fully associative instruction cache using LRU replacement.

    a. Explain how this would be possible (*Hint:* You can't explain this with the three C's model because it "ignores" replacement policy)
    b. Explain where replacement policy fits into the three C's model, and explain why this means that misses caused by a replacement policy are "ignored"- or, more precisely, cannot in general be definitively classified by the three C's model.
    c. Are there any replacement polices for the fully associative cache that would outperform the direct-mapped cache? Ignore the policy of "do what a direct- mapped cache would do".
    d. Use a cache simulator to see if Smith and Goodman's results hold for memory reference traces that you have access to. If they do not hold, why not?

2. John takes two numbers in sign magnitude representation (the two numbers are same with different signs), The 1's complement of one number is 6. The difference between 1's complement of these two numbers is 32. Find the numbers. And also find the product of these two numbers using the result of 2's complement value of these two numbers.

Analyze

1. A two-word instruction is stored in memory at an address designated by the symbol W. The address field of the instruction (stored at W + 1) is designated by the symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from the other addresses if the addressing mode of the instruction is a. direct b. indirect c. relative d. indexed.
2. An 8-bit computer has a 16-bit address bus. The first 15 lines of the address are used to select a bank of 32K bytes of memory. The high-order bit of the address is used to select a register which receives the contents of the data bus. Explain how this configuration can be used to extend the memory capacity of the system to eight banks of 32K bytes each, for a total of 256K bytes of memory.

21EC505 Linear IC Applications Lab

0 0 3 1.5

Course Outcomes:

1. Design Linear and nonlinear applications of OP-AMP
2. Implement Active Filters using IC 741
3. Design Waveform generators using IC 741 and 555 timers
4. Implement A/D and D/A convertors
5. Design PLL applications and voltage regulators
6. Implement Real time applications by using OP-AMP and 555 Timer

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PSO_1
1	3	2	2	2	3
2	3	2	2	2	3
3	3	2	2	2	3
4	3	2	2	2	3
5	3	-	2	2	3
6	3	3	3	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

List of Experiments
Students will perform minimum twelve Experiments

1. Inverting and Non-inverting Amplifiers using Op Amps.
2. Adder and Subtractor using Op Amp.
3. Comparators and voltage Follower using Op Amp.
4. OP AMP Applications–differentiator, integrator circuit
5. Square wave and Triangular waves generator using OP-AMP
6. Schmitt Trigger Circuit–Using IC 741
7. Astable multivibrator using IC 741
8. Active Filters–LPF, HPF (first order only)
9. Active Filter–Band Pass Filterand Band Reject Filter
10. IC 555 Timer– Monostable Operation Circuit
11. IC 555 Timer- Astable Operation Circuit
12. IC 565 – PLL Applications.
13. RC Phase Shift using IC-741 Op-Amp
14. Voltage Regulator using IC 78XX,79XX, 723
15. Analog to Digital Converter using OP AMP
16. Digital to Analog Converter using OP AMP

List of Augmented Experiments*

1. Design a function generator to generate sine wave, square wave and triangular wave range from 1KHz to 1MHz
2. Design a filter eliminate the noise from ECG
3. Design a Mosquito repeller by using 555 Timers
4. Design a calling bell circuit which produce Ding-Dong Soundby using 555 timer

Reading Material(s)

1. Ramakanth A. Gayakwad, Op-Amps & Linear ICs, PHI, 4th Edition. 2002.
2. D. Roy Chowdhury,Linear Integrated Circuits, New Age International (p) Ltd, 2nd Edition,2003.
3. LICA lab Manual.

21TPX01 Term Paper

0 0 3 1.5

Course Outcomes

1. Interpret the literature to link the earlier research with the contemporary technologies
2. Communicate effectively as an individual to present ideas clearly and coherently
3. Review the research findings and its correlation to the latest applications
4. Prepare documents and present the concepts clearly and coherently
5. Inculcate the spirit of enquiry for self-learning
6. Identify interdisciplinary oriented topics

COs – POs Mapping

COs	PO1	PO4	PO10	PO12
1	-	2	-	-
2	-	-	3	3
3	3	-	-	-
4	-	-	3	-
5	-	-	-	3
6	1	-	-	-

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

21ESX02 Employability Skills II

0 0 2 0

Course Outcomes

1. Demonstrate oral communication and writing skills as an individual to present ideas coherently
2. Develop life skills with behavioral etiquettes and personal grooming.
3. Assess analytical and aptitude skills.
4. Develop algorithms for engineering applications.
5. Solve engineering problems using software.
6. Utilize simulation tools for testing.

COs – POs Mapping

COs	PO1	PO2	PO5	PO8	PO10	PO12
1					3	2
2				1	2	2
3	2	1		2		
4	2		2			
5	2		2			
6	2		2			

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

1. Communication Skills, Confidence and Quantitative Aptitude

Introduction to Campus Placements: Stages of Campus Placement, Skills assessed in Campus Placements & How to get ready?

Motivational Talk on Positive Thinking: Beliefs, Thoughts, Actions, Habits & Results (Success)

Resume Preparation: Resume? Templates? Mistakes to be avoided in a Resume, Steps to be followed in preparing it.(with examples)

Group Discussions (Recap): GD? Stages of a GD, Skills assessed in a GD, Blunders to be avoided, How to excel in a GD? (through Practice Sessions)

Psychometric Tests: Definition, Types of Psychometric Tests: Numerical Computation, Data Interpretation, Verbal Comprehension, Verbal Critical Reasoning and Personality Questionnaires

Exercises related to Communication: Story Writing, TAT etc

7Hours

2. Quantitative Aptitude

Square &Cube roots, Partnership, Logarithms, Progressions, Mensuration, Data Sufficiency

8 Hours

Unit II

DATA FLOW LEVEL

Continuous assignment structures, Delays, and Continuous assignments, Assignment to Vectors, Operators, Strength contention with Tri-reg Nets.

Practical Components

1. Perform the simulation of full adder and half subtractor using data flow modelling in Verilog HDL.
2. Perform the Dataflow modeling for multiplexer and demultiplexer in Verilog HDL.
3. Perform the Dataflow modelling for 3 to 8 decoder in Verilog HDL.
4. Perform the Dataflow modelling for n-bit Johnson counter in Verilog HDL.
5. Perform the simulation of parity bit generation using data flow modelling in Verilog HDL.
6. Perform the Dataflow modelling for 8-bit adder in Verilog HDL.
7. Perform the Dataflow modelling for n-bit right-to-left shift register in Verilog HDL.
8. Perform the Dataflow modelling for BCD addition in Verilog HDL.
9. Perform the Dataflow modelling for JK flipflop and T-flip flops in Verilog HDL.

15 Hours

Total 30 Hours

Textbook (s)

1. Padmanabhan, Tattamangalam R., and B. Bala Tripura Sundari. Design Through Verilog HDL. John Wiley & Sons, 2003.

Reference (s)

1. Palnitkar, Samir. *Verilog HDL: a guide to digital design and synthesis*. Vol. 1. Prentice Hall Professional, 2003.
2. Ciletti, Michael D. *Advanced digital design with the Verilog HDL*. Vol. 1. Upper Saddle River: Prentice hall, 2003.

21HSX12 CC & EC Activities II

0 0 1 0

Course Outcomes

1. Interpret and present the abstractive technical information through an activity
2. Think critically in providing solutions to the generic and common problems
3. Demonstrate the creative thinking in dealing with liberal arts
4. Instill team sprit through active engagement with the peer
5. Develop programs of common interest having social impact
6. Empower the under privileged through motivational activities

COs – POs Mapping

COs	PO6	PO7	PO9	PO10
1	-	-	-	3
2	3	2	-	-
3	3	-	-	-
4	-	-	3	-
5	3	-	-	-
6	3		-	-

21SIX01 Summer Internship I

0 0 0 1

Course Outcomes

1. Demonstrate the application of knowledge and skill sets acquired from the course and workplace in the assigned job function/s
2. Solve real life challenges in the workplace by analyzing work environment and conditions, and selecting appropriate skill sets acquired from the course
3. Articulate career options by considering opportunities in company, sector, industry, professional and educational advancement
4. Communicate and collaborate effectively and appropriately with different professionals in the work environment through written and oral means
5. Demonstrate the ability to harness resources by examining challenges and considering opportunities
6. Demonstrate appreciation and respect for diverse groups of professionals by engaging harmoniously with different company stakeholders

COs – POs Mapping

COs	PO1	PO2	PO8	PO10	PO12
1	3	-	-	-	-
2	3	-	-	-	-
3	-	-	-	-	3
4	-	-	-	3	-
5	-	2	-	-	-
6	-	-	3	-	-

21HSX10 Engineering Economics and Project Management

3 0 0 3

Course Outcomes

1. Illustrate the basic principles of engineering economics.
2. Demonstrate Cost-Volume-Profit (CVP) analysis in business decision making.
3. Implement the simple financial statements for measuring financial performance of a firm.
4. Evaluate investment proposals through various capital budgeting methods.
5. State key issues of organization, management and administration.
6. Determine the accurate project cost estimates and plan future activities.

CO-PO Mapping

CO_s	PO_{10}	PO_{11}	PO_{12}
1	1	1	2
2	3	2	1
3	3	3	2
4	2	2	1
5	1	2	1
6	2	3	1

3–Strongly linked | 2–Moderately linked | 1–Weakly linked

Unit I

Introduction to Engineering Economics - Demand Forecasting & Cost Analysis

Concept of Engineering Economics – Types of efficiency – Managerial Economics Nature and Scope – Law of Demand – Types of Elasticity of demand.

Demand Forecasting & Cost Analysis: Demand Forecasting: Meaning, Factors Governing Demand Forecasting, Methods of Demand Forecasting (Survey and Statistical Methods) – Cost Analysis: Basic Cost Concepts, Break Even Analysis.

Factors affecting the elasticity of demand – Supply and law of Supply **11 Hours**

Unit II

Market Structures - Financial Statements & Ratio Analysis

Different type of Markets Structures – Features – Price Out-put determination under Perfect Competition and Monopoly

Financial Statements & Ratio Analysis: Introduction to Financial Accounting – Double entry system – Journal – Ledger – Trail Balance – Final Accounts (with simple adjustments) – Financial Analysis through Ratios: Interpretation of Liquidity Ratios (Current Ratio and quick ratio), Activity Ratios (Inventory turnover ratio and Debtor Turnover ratio, Creditors Turnover Ratio, Capital Turnover Ratio), Solvency Ratios (Debt- Equity ratio, Interest Coverage ratio), and Profitability ratios (Gross Profit Ratio, Net Profit ratio, Operating Ratio, P/E Ratio and EPS).

Price output determination under Monopolistic markets, Accounting concepts and conventions **13 Hours**

Unit III

Investment Decisions and Fundamentals of Management

Time Value of Money – Capital Budgeting: Meaning, Need and Techniques of Capital Budgeting

Introduction to Management: Nature – Importance – Classical Theories of Management: F.W.Taylor's and Henri Fayol's Theory – Functions and Levels of Management – Decision Making Process – Inventory Control, Objectives, Functions – Analysis of Inventory – EOQ.

Maslow & Douglas McGregor theories of Management, ABC Analysis **12 Hours**

Unit IV

Project Management

Introduction – Project Life Cycle and its Phases – Project Selection Methods and Criteria – Technical Feasibility – Project Control and Scheduling through Networks – Probabilistic Models of Networks – Time-Cost Relationship (Crashing) – Human Aspects in Project Management: Form of Project Organization – Role & Traits of Project Manager.

Sources of Long-term and Short-term Project Finance **12 Hours**

Total: 48 Hours

Textbook (s)

1. Pravin Kumar, Fundamentals of Engineering Economics, Wiley India Pvt. Ltd. New Delhi, 2015
2. Rajeev M Gupta, Project Management, 2nd Ed., PHI Learning Pvt. Ltd. New Delhi, 2014

Reference (s)

1. Panneer Selvam. R, Engineering economics, 2nd Ed.,, Prentice Hall of India, New Delhi, 2013
2. R.B.Khanna, Project Management, PHI Learning Pvt. Ltd. New Delhi, 2011
3. R. Panneer Selvam & P.Senthil Kumar, Project Management, PHI Learning Pvt. Ltd. New Delhi, 2010
   A. Aryasri, Management Science, 4th Ed., Tata McGraw Hill, 2014
   A. Aryasri, Managerial Economics and Financial Analysis, 4th Ed., Tata McGraw Hill, 2014
4. Koontz & Weihrich, Essentials of Management, 6th Ed., TMH, 2010
5. Chuck Williams and Mukherjee, Principle of Management 7th Ed., Cengage Learning, 2013

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	25	25	--
Understand	35	35	--
Apply	40	40	50
Analyze	--	--	50
Evaluate	--	--	-
Create	--	--	--
Total (%)	100	100	100

Remember

1. Define Managerial Economics. Explain its nature and scope.
2. Define Production Function? List the various types of production functions
3. Define the meaning of productivity? Explain how productivity can be enhanced in the Indian industries.
4. Define management and its functions
5. List out short-term source of finance and explain briefly
6. Why is it essential to define project life cycle and divide it into various phases?

Understand

1. Summarize engineering economics with suitable examples.
2. Explain different elements of costs used in cost analysis
3. Illustrate the effect of price on demand and supply with the help of a diagram.
4. Explain the features of Perfect Competition
5. Describe the Top level Upper Middle level of management and its functions
6. Explain Price-Output determination under Perfect Competition under Market period

Apply

1. Consider the following data of company for the year 2015
   Sales = Rs.2,40.000/-
   Fixed cost = Rs.50,000/-
   Variable cost = Rs.75,000/-
   Find out the followings
   a) Profit b) BEP c) Margin of safety
2. The following trial balance of Mr. Ramesh, prepare trading, profit & loss A/c for the year ended 31.12.2018 and balance sheet as on that date.

Particulars	Debit (Rs.)	Credit (Rs.)
Capital		1,00,000
Drawing	18,000	
Furniture	32,500	
Machinery	15,000	
Bills payable		15,000
Interest paid	900	
Sales		1,00,000
Purchases	75,000	
Opening stock	25,000	
Advertisement	15,000	
Wages	2,000	

Insurance	1,000	
Commission received		4,500
Sundry debtors	28,100	
Cash in hand	20,000	
Sundry creditors		10,000
Interest received		3,000
Total	**2,32,500**	**2,32,500**

Adjustments:

Closing Stock Rs.60,000 b) Outstanding wages Rs.500

3. From the following balances as on the date March 31st, 2014.

Particulars	Amount (Rs.)	Particulars	Amount (Rs.)
10% Debentures	3,00,000	Cash in hand	30,000
6% Long term Loans	50,000	Debtors	15,000
Share capital	2,50,000	Opening stock	50,000
Creditors	1,00,000	Closing stock	40,000
Bill payable	45,000	Gross Profit	20,000
Sales	100000	Building	700000

Calculate: Current Ratio, Debt-equity ratio, Quick ratio, Inventory turnover ratio, Debtors turnover ratio

4. A company requires 40,000 kg of raw materials. The company incurs a handing cost of Rs.360/- plus freight of Rs.390 per order. The incremental carrying cost of inventory of raw material is Rs. 15 per kg. Calculate:
   a) EOQ b) Number of orders per annum c) How frequently should orders be placed
5. The following table gives the activities in a construction project and other related information:

Activity	Immediate Predecessors	t_0	t_m	t_p
A	-	1	9	11
B	-	5	6	7
C	A	5	7	9
D	A,B	4	7	10
E	C,D	1	4	7
F	C,D	7	9	11

a) Draw PERT diagram
b) Calculate total project duration
c) Mark the critical path
d) Find out the S.D and Variance of each activity

6. ABC Ltd., a US based organization, is engaged in manufacturing television screens. It is planning to establish a subsidiary organization in India to manufacture picture tubes. Cost studies produced the following estimates for the Indian subsidiary based on the estimated annual sales of picture tube (Rs.400000/-):

Particulars	Total Annual Cost (Rs.)	Percent of total annual cost that is variable
Materials	1936000	100%
Labour	900000	70%
Overhead	800000	64%
Administration	300000	30%

The Indian production would be sold by manufacturer's representatives who would receive a commission of 8% of the sales. No portion of the parent organizations' expenses is to be allocated to the Indian subsidiary.

Questions:

1. Compute the sale price per picture tube to enable management to realize an estimated 10% profit on sale proceeds in India.
2. Is it feasible for ABC Ltd., to invest in the Indian market by studying the preceding calculation? **(For Open Book Examination and not for semester end examination)**

Analyze:

1. From the following cases analysis the situation of price elasticity of product.

Case 1:

Price of product (Rs.)	Quantity of Demand (Units)
100	1000
90	1500

Case 2:

Price of product (Rs.)	Quantity of Demand (Units)
100	1000
70	1100

2. Analyze the attributes to be consider for selection project
3. Differentiate between Perfect Competition & Monopoly Competition
4. Compare significances and limitation of liquidity and solvency ratios.
5. You are given the following information about two companies in the year 2020.

Particular	Company – A	Company – B
Sales	Rs. 50,00,000	Rs. 50,00,000
Fixed Expenses	Rs. 12,00,000	Rs. 17,00,000
Variable Expenses	Rs. 35,00,000	Rs. 30,00,000

A friend seeks your advices as to which company's shares be should purchase. Assuming the capital invested is equal for the two companies, state the advice that you will give.

6. A private school is considering the purchase a school bus to transport students to school. The initial cost of the bus is Rs.600,000. The life of bus is estimated to be five years, after the life time the vehicles would have to be scrapped with no salvage value. The school's management team has derived the following estimates for annual revenues and cost for the next five years.

year	Annual Revenue	Diver Cost	Repairs & maintenance	Other costs	Annual depreciation
1	330000	33,000	8,000	130000	120000
2	330000	35,000	13,000	135000	120000
3	350000	36,000	15,000	140000	120000
4	380000	38,000	16,000	136000	120000
5	400000	40,000	18,000	142000	120000

The buses would be purchased at the beginning of the project (i.e., in Year 0) and all revenues and expenditures shown in the table above would be incurred at the end of each relevant year. A business consultant has advised management that they should use a cost of capital of 10% to evaluate this project.

Questions:

1. Attributes to be involved to estimate the net cash flow for each year in this project.
2. Justify the steps involved in the calculation process of net present cash flows above the project investment. **(For Open Book Examination and not for semester end examination)**

21EC601 Cellular and Mobile Communications

3 0 0 3

Course Outcomes

1. Summarize basic cellular system, handoff, frequency reuse and improving capacity of cellular system
2. Demonstrate various interference types, frequency management and channel assignment
3. Interpret various cell site and mobile antennas
4. Outline the phase difference, propagation effects in various cell coverage environments
5. Assess the Multiple access schemes and GSM digital cellular system
6. Outline the 4G cellular technology

COs–POs Mapping

COs	PO_1	PO_2	PSO_2
1	2	-	2
2	3	2	3
3	2	-	2
4	3	2	3
5	3	2	3
6	3	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Introduction to Cellular systems and Co-Channel Interference

Introduction to cellular mobile system, Evolution of cellular systems, Performance criteria, Basic cellular system, concept of frequency reuse, Trunking and Grade of Service, Improving capacity of cellular systems: Cell splitting, Sectoring, Micro cell concept, Handoff and dropped calls. Co-Channel Interference reduction factor, Desired C/I calculation for Omni directional and directional antenna systems.

Repeaters for range extension, Picocell zone concept

12 Hours

Unit II

Frequency Planning and Cell Site- Mobile Antennas

Adjacent channel interference: Next channel and neighboring channel interference, Frequency management: Numbering, grouping of channels, channel types, channel assignment: fixed channel assignment, non-fixed channel assignment. Cell Site and Mobile Antennas: Omni directional antennas, Directional antennas for interference reduction, space diversity antennas, and Umbrella pattern antennas, minimum separation of cell site antennas, roof mounted and glass mounted antennas, high gain antennas.

Interference in heterogeneous network, Effect of lowering the antenna height

12 Hours

Unit III

Cell coverage and Multiple access schemes

Cell coverage for signal and traffic**:** Signal reflections in flat and hilly terrain, effect of human made structures, phase difference between direct and reflected paths, constant standard deviation, straight line path loss slope, general formula for mobile propagation over water and flat open area, foliage loss, near and long distance propagation, antenna height gain, form of a point to point model, cell site antenna heights and signal coverage cells. Multiple access schemes: TDMA, FDMA and CDMA

Near and long distance propagation, WCDMA Architecture

13 Hours

Unit IV

Digital Cellular Systems and 4G Technology

Digital Cellular system: GSM Architecture, GSM operation, Channels and frame structure for GSM. Evolution of 4G: Objectives and advantages, 4G Technologies: Ultra Wide band network, OFDM and MIMO antenna systems.

GSM protocols, Limitations of 4G

11 Hours

Total: 48 Hours

Textbook (s)

1. W.C.Y. Lee, Mobile Cellular Telecommunications, Tata McGraw Hill, 2nd Edition, 2006
2. Theodore. S. Rapport , Wireless Communications, Pearson education, 2nd Edition., 2002.
3. Gottapu Sasibhushana Rao, Mobile Cellular Communication, Pearson International, 2012

Reference (s)

1. D.Tse and P.Viswanath, Fundamentals of wirless communication, Cambridge University press, 2005.
2. W.C.Y.Lee , Wireless and Mobile Communications, McGraw Hill, 3rd Edition, 2006.

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	20	15	--
Understand	50	50	--
Apply	30	35	60
Analyze	-		40
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. State two reasons for choosing 800MHz band for mobile radio systems.
2. List two disadvantages of conventional mobile system.
3. List two major approaches to achieve the ideal mobile telephone system.
4. Define multipath fading.

Understand

1. Represent grade of service.
2. Abstract the term co-channel interference.
3. Identify the major functions of MTSO.

Apply

1. Demonstrate cell splitting and types of cell splitting.
2. Demonstrate Handoff techniques.
3. Assess the frequency reuse concept of cellular systems.

[Open Book Examination Questions]

1. Find the frequency reuse factor and the cellular size that should be used for maximum capacity if the path-loss exponent is
   $\lambda = 4$
   $\lambda = 2$
   a. Assume that there are six co-channel cells in the first tier and all of them at the same distance of $D + 0.7R$ from the mobile. Use suitable approximations. If carrier-to-noise interference ratio of 20 dB is required for a satisfactory forward channel performance of a cellular system.

2. Compute the number of channels available in an FDMA system in such a way that an AMPS cellular operator is allocated with 15 MHz for each simplex band, and if B_t is 15 MHz, B_g is 15 KHz, and B_c is 30 KHz.

Analyse

1. Justify the effect of lowering the antenna height on interference in a valley.
2. Compare the C/I worst case for K=4 and K=7 pattern cellular systems.
3. Outline the limitations of conventional mobile systems and spectrum efficiency considerations.
4. Compare sectoring and micro cell zone concept.

[Open Book Examination Questions]

1. Breakdown all physical circumstances that relate to a stationary transmitter and a moving

receiver such that the Doppler shift at the receiver is equal to

i) 0 Hz
ii) f_{dmax}
iii) $-f_{dmax}$

3. Conclude the major factors causing propagation path loss and compare large-scale propagation path-loss models and small-scale propagation path-loss models in detail.
4. Compare the features of various wireless networks starting from 1G to 4G technologies (OBE).
5. Outline the salient features of wireless technology in the development of next generation cellular communication systems.

21EC602 Digital Signal Processing

3 0 0 3

Course Outcomes

1. Classify discrete time signals and systems
2. Implement Digital systems by using realization techniques
3. Implement discrete Fourier transform and Fast Fourier transform on time domain signals
4. Differentiate FIR and IIR digital filters
5. Demonstrate the concept Multirate signal processing
6. Interpret the architecture of Digital signal processors

COs – POs Mapping

COs	PO_1	PO_2	PSO_2
1	2	-	2
2	3	2	3
3	3	2	3
4	3	2	3
5	3	2	3
6	2	-	2

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Introduction to Discrete–Time signals and systems

Classification of Discrete time signals, linear Time Invariant systems, stability, and causality, Linear convolution in time domain and graphical approach, Frequency Domain Representation of Discrete-Time Signals and systems. Concept of Z-transforms, Region of Convergence, properties, Inverse Z transform, Realization of Digital filter structures: Direct form-I, Direct form-II, Transposed form, Cascaded form, Parallel form

Lattice structure, Lattice-Ladder structure **12 Hours**

Unit II

Discrete–Time signals in Transform domain

Discrete Fourier Series(DFS),Discrete Time Fourier transforms(DTFT), Discrete Fourier transform(DFT), Properties of DFT , linear convolution using DFT, Circular convolution, Fast Fourier transforms (FFT) - Radix-2 decimation in time ,decimation in frequency FFT Algorithms, Decimation in frequency FFT Algorithms, Inverse FFT, Overlap-save method, Overlap-add method

Relation between DTFT, DFS, DFT, Radix-4FFT

12Hours

Unit III

IIR &FIR Digital Filters

Analog filter approximations–Butter worth and Chebyshev, Impulse Invariant transformation, Bilinear transformation, Design of IIR Digital filters from analog filters, FIR Digital Filters: Characteristics of FIR Digital Filters, frequency response, Design of FIR Digital Filters using Window Techniques, Frequency Sampling Technique.

Comparison of IIR & FIR filters. Frequency Transformation in digital domain,

13 Hours

Unit IV

Multirate Signal Processing & TMS Processors

Multirate Processing: Decimation, interpolation, sampling rate conversion, Implementation of sampling rate conversion. Introduction to DSP processors: Overview of Digital signal processors, Von Neumann Architecture, Harvard Architecture, Multiplier Accumulator (MAC), Pipelining, Architecture of TMS320C50,Bus structure, CPU, on chip memory, on-chip peripherals

Cascading sampling rate converters, Addressing modes

11Hours

Total: 48 Hours

Textbook (s)

1. Digital Signal Processing by Sanjit K.Mitra 2nd Edition , TATA McGraw Hill

2. John G. Proakis, Dimitris, G.Manolakis ,Digital Signal Processing, Principles, Algorithms, and Applications: Pearson Education / PHI, 4th Edition, 2013.
3. Digital Signal Processors – Architecture, Programming and Applications,, B.Venkataramani, M. Bhaskar, TATA McGraw Hill, 2002

Reference (s)

1. SanjitK.Mitra, Digital Signal Processing, Tata Mc Graw Hill publishers, 3rd Edition, 2009.
2. Alan V. Oppenheim, Ronald W. Schafer Digital Signal Processing, PHI, 4th Edition, 2007
3. Andreas Antoniou, Digital Signal Processing, TATA McGraw Hill , 2006
4. MH Hayes, Digital Signal Processing, Schaum's Outlines, Tata Mc-Graw Hill, 2007

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	25		--
Understand	35	25	--
Apply	20	45	60
Analyse	20	30	40
Evaluate	--		--
Create	--		--
Total (%)	100	100	100

Remember

1. Define Signal and System.
2. State the advantages and limitations of DSP?
3. Define about Gibb's phenomena
4. state the need of Multi rate signal processing
5. List the difference between FIR and IIR filters

Understand

1. Identify the following systems for time invariant
   (i) $y(n) = x(n) - x(n-1)$
   (ii) $y(n) = nx(n)$
   (iii) $y(n) = e^{x(n)}$
2. Identify the stability of the given systems
   (i) $y(n) = \cos(x(n))$
   (ii) $y(n) = x(-n-2)$
   (iii) $y(n) = ax^2(n)$
3. Illustrate whether the signal x(n)=sin15πn+ sin√2_n is periodic or not.
4. Illustrate windowing techniques to design FIR filters.
5. Represent y(n)=x(n)+2x(n-1)+3x(n-2)+2y(n-1)+3y(n-2) in direct form-**I** structure.

Apply

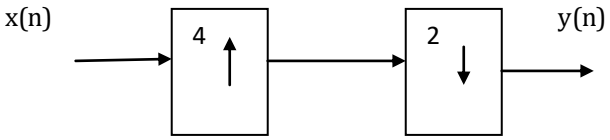
1. Realize the system given by the difference equation y(n)= -0.1y(n-1)+0.72y(n-2)+0.7x(n)-0.252x(n-2) in parallel form.

2. Find the DFT of a sequence x[n] = {1, 2, 3, 4, 4, 3, 2, 1}using DIT algorithm

3. Compute the IDFT of the sequence X[k] = {12, 0, 0, 0, 4, 0, 0, 0} using DIF Algorithm

[Open Book Examination Questions]

4. A DSP system is characterized by linear difference equation $y(n) = 2x(n) + 4x(n-1) + 6x(n-2) + 8x(n-3)$ with digital input $x(n) = \{1,0,1,1\}$. Find the output response of the system.Find the transfer function of FIR system
   [Open Book Examination Questions]
5. Show the expression for the output in terms of x(n) for the multi rate system given as follows



[Open Book Examination Questions]

Analyse

1. Resolve analog filter with transfer function $(s+0.1)/(s+0.1)^2+9$, into a digital IIR filter using bilinear transformation. The digital filter should have a resonant frequency of $\omega_r = \pi/4$

2. The specification of the desired LPF is
   Design a Butterworth IIR digital filter using Impulse invariant transformation technique

$$0.8 \le |H(\omega)| \le 0.1 \qquad 0 \le \omega \le 0.2\pi$$
$$|H(\omega)| \le 0.2 \qquad 0.32\pi \le \omega \le \pi$$

3. Compare the frequency response of Linear phase FIR filter
   Case(1) impulse response $h_{(n)}$ is symmetrical N is odd
   Case(2) impulse response $h_{(n)}$ is anti symmetrical N is even
   Case(3) impulse response $h_{(n)}$ is symmetrical N is even
   Case(4) impulse response $h_{(n)}$ is anti-symmetrical N is odd
   [Open Book Examination Questions]
4. Outline the structural realization of linear phase FIR filter for given N
   Case(1) h(n) = {3 2 1 2 3} for N=5
   Case(2) h(n) = {-3 -2 0 2 3} for N=5
   Case(3) h(n) = {3 2 1 1 2 3} for N=6
   Case(4) h(n) = {-3 -2 -1 1 2 3} for N=6
   [Open Book Examination Questions]
5. Compare different windowing techniques
   [Open Book Examination Questions]

21ECC12 ASIC Verification using System Verilog

3 0 2 4

Course Outcomes

1. Interpret the verification guidelines and data types
2. Execute the programs using assertions and Routines.
3. Demonstrate the System Verilog constructs through simulations
4. Explain the basic OOPs concepts.
5. Organize the design modules in SV test bench.
6. Exemplify the ASIC verification using SV testbench

COs – POs Mapping

COs	PO1	PO2	PO3	PO4	PO5	PSO1
1	2	2	1	2	3	2
2	3	2	2	2	3	3
3	3	2	2	2	3	3
4	2	2	1	2	3	2
5	3	2	2	2	3	3
6	3	2	2	2	3	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Introduction to Verification and Data Types

Introduction to the functional verification Process, The Verification Methodology, Basic Test-bench Functionality, Directed Testing, Constrained-Random Stimulus, Functional Coverage, code coverage, Test-bench Components, Layered Test-bench, Simulation Environment Phases.

Introduction to data types, Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Associative Arrays, Array Methods, Creating New Types with typedef, Creating User-Defined Structures, Enumerated Types, Constants, Strings, Net Types, Time Scale.

String methods, operators

Practical Components

1. Develop an SV module to demonstrate the declaration of variables
2. Develop a system Verilog code to demonstrate the declaration & application of packed and unpacked arrays.
3. Develop an SV module to demonstrate the application of Ques and simulate
4. Develop a System Verilog program to create two dynamic arrays, insert an elements and display the size.

13+8 Hours

Unit II

Assertions and Routines

Introduction, Assertions: Immediate assertions, Concurrent assertions, Example programs for assertions, Tasks, Functions, Void Functions, Automatic functions, Routine Arguments, Time Scale, System tasks.

Enumerated types, repeat and forever

Practical Components

1. Develop a system Verilog code to demonstrate Immediate assertions
2. Develop a System Verilog testbench to demonstrate the Concurrent assertions
3. Develop a System Verilog test bench to differentiate the calling of a task and a function
4. Develop a System Verilog test bench to demonstrate the passing arguments by value & by reference to a function

11+8 Hours

Unit III

Basic OOPs

Introduction, OOP Terminology, Creating New Objects, Object Deallocation, Using Objects, Static Variables vs. Global Variables, Class Routines, Defining Routines Outside of the Class, Scoping Rules, Using One Class Inside Another, Understanding Dynamic Objects, Copying Objects.

Nested–Inner Class & Anonymous Classes–Generic Class Types

Practical Components

1. Develop an SV module to demonstrate the declaration of objects and classes
2. Write a System Verilog code to demonstrate the derived class to refer to members of the parent class.
3. Develop an SV module to demonstrate the inheritance
4. Develop an SV module to demonstrate the shallow copy to generate the different instances of a class

12+8 Hours

Unit IV

Connecting the Test bench and Design

Introduction to Universal verification methodologies (UVM), Interface: connecting the interface with DUT, Interface parametrization, Interface Driving and Sampling, Case study of Layered testbench: A testbench composed with transaction object, Generator, Driver, Monitor, Scoreboard, Environment, Test case, Interface. EDA tools for the design verification.

Inter process communication: semaphore, mailboxes and event

Practical Components

1. Write a System Verilog program to demonstrate interface
2. Develop a test bench in SV to test a Sequence detector and simulate
3. Develop an SV module to demonstrate the verification of a simple adder using a layered testbench
4. Explore an EDA Development Environment

12+8 Hours

Total: 48+32 Hours

Textbook (s)

1. Chris Spear, "System Verilog for Verification: A Guide to Learning the Test bench Language Features", Springer-Verlag New York, Inc. Secaucus, NJ, USA, 2006
2. Donald Thomas, "Logic Design and Verification Using System Verilog", Create Space Independent Publishing Platform, 2014.

Reference (s)

1. Language Reference Manual for System Verilog

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Lab Examination (%)
Remember	--	--	--
Understand	50	50	--
Apply	50	25	100
Analyze	--	25	--
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

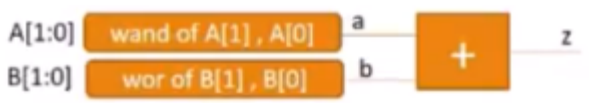
1. Define transaction level modelling.
2. What are the different types of data types in system Verilog
3. What is the need of clocking blocks
4. Describe the difference between code coverage and functional coverage

Understand

1. Distinguish between functions and tasks in system Verilog using a suitable example
2. Explain the use of fork/join in system Verilog with a suitable example
3. What are the different semaphore methods in SV , write a semaphore example

Apply

1. Take 2 bits vector A and B , write a SV code that verifies all the possibilities of below block diagram, example –A=2'B01, B=2'bXZ, z=? Verify a,b with wand, wor truth-table, respectively.



2. Write a program to explain polymorphism in system Verilog.
3. Write a program to create a system Verilog interface.

21ECC22 Embedded System Design and IoT

3 0 2 4

Course Outcomes

1. Interpret embedded system architecture
2. Demonstrate embedded target boards and firmware development
3. Demonstrate interfacing of IO devices
4. Illustrate various IoT characteristics and architectures
5. Assess real world parameters for IoT applications
6. Design prototype embedded systems using IoT

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PO_5	PSO_1
1	2	-	-	-	-	2
2	3	2	2	2	3	3
3	3	2	2	2	3	3
4	2	-	-	-	-	2
5	3	2	2	2	3	3
6	3	2	2	2	3	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Introduction to Embedded Systems

Definition, Embedded system versus general Computing Systems, Quality Attributes of Embedded Systems, The typical Embedded System, core of Embedded System, Memory, sensors and actuators, Communication Interface, Embedded Firmware, other system components, On board and off board communication interfaces: *UART,* I2C, SPI, BLUE TOOTH, WIFI. Embedded target boards: Arduino board, Raspberry pi.
ZIGBEE, USB

Practical Components

1. Blinking of LED using embedded target board.
2. Traffic system Controller
3. Interfacing of seven-segment display with embedded target board.

12+6 Hours

Unit II

Hardware and firmware development

Embedded firmware design approaches and development languages, Embedded C, Fundamental Issues in Hardware and Software Co-Design, Hardware software tradeoffs, Integration of Hardware and Firmware. CAD and hardware Translation tools. Pre-processors, Interpreters, Compilers, Linkers. Debugging tools, Simulators and Laboratory tools.
Emulator, beagle bone embedded target board

Practical Components

1. Interfacing of dc motor with embedded target board and controlling it's speed using PWM concept.
2. Interfacing of LCD with embedded target board.
3. Interfacing of keypad with embedded target board.
4. Interfacing of high voltage device using relay with embedded target board.

12+8 Hours

Unit III

IoT Architecture and Data Analytics

IoT characteristics and Applications, M2M vs. IOT, M2M Value Chains, IoT Value Chains, The international driven global value chain and global information monopolies. Functional View, Information View, Deployment and Operational View, Other Relevant architectural views, sensing the real world for IoT applications, temperature sensor, humidity and temperature sensor, light dependent register, touch sensor, smoke detector, rain detector, ultrasonic sensor, soil moisture sensor.
LoRa Wan and 6lowpan

Practical Components

1. Interfacing of light dependent register with embedded target board.
2. Interfacing of touch sensor with embedded target board.
3. Interfacing of smoke detector with embedded target board.
4. Interfacing of rain detector with embedded target board.
5. Interfacing of ultrasonic sensor with embedded target board.

12+10 Hours

Unit IV

IoT web Services and business Applications

Introduction to ESP8266 Wi-Fi module, Node MCU Development board, various Wi-Fi library, web server-introduction, installation, configuration, posting sensor(s) data to web server, cloud platforms for IOT, virtualization concepts and cloud architecture, cloud computing, benefits, cloud services - SaaS, PaaS, IaaS, cloud providers & offerings, study of IOT cloud platforms, thing speak API and MQTT, IoT Application : city automation, automotive applications, home automation, process monitoring / automation, smart transportation, smart metering, smart waste management system.

IoT for smart grid, smart healthcare

Practical Components

1. Configure Thingspeak cloud platform for displaying real-time temperature.
2. Configure Blynk cloud platform for turning on/off.
3. Interfacing of humidity and temperature sensor (DHT11) with embedded target board.
4. Interfacing of temperature sensor (LM35) with embedded target board.

12+08 Hours

Total: 48+32 Hours

Textbook (s)

1. Shibu .K.V, Introduction to Embedded Systems, 1st Ed, Tata McGraw Hill Education Private Limited, 2009.
2. Yogesh Misra, Programming and Interfacing with Arduino, CRC Press, 1st Edition, 2021
3. Daniel Minoli, Building the Internet of Things with IPv6 and MIPv6: The Evolving World of M Jan Holler, Vlasios Tsiatsis, Catherine Mulligan, Stefan Avesand, Stamatis Karnouskos, David
4. Rajkamal, Internet of things: Architecture and design principles, TMH Publication, 2017

Reference (s)

1. Tammy Noergaard , Embedded systems Architecture, Elsevier publications, 2005
2. Michael Margolis, "Arduino Cookbook", First Edition, March 2011, O'Reilly Media, Inc
3. Boyle, From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence, 1st Edition, Academic Press, 2014.2M Communications, ISBN: 978-1-118-47347-4, Willy Publications, 2014

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Lab Examination (%)
Remember	25	25	--
Understand	30	30	--
Apply	45	45	100
Analyze	--	--	--
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. Define embedded system.
2. List any three on board and off board communication interfaces.
3. Recall the microcontroller used in Arduino UNO board.
4. List any two embedded development boards.

Understand

1. Exemplify the SPI protocol for on board communication interface.
2. Exemplify the I2C protocol for on board communication interface.
3. Demonstrate the purpose of compiler and linker in firmware design.
4. Illustrate the different components of Arduino UNO board.
5. Illustrate the working of capacitive touch sensor.

Apply

1. Construct an interfacing diagram of LCD with Arduino board and develop the software to display a message from the 5th row and 2nd column of LCD.
2. Construct an interfacing circuit of 220 V ac operated bulb with Arduino board and develop the software to turn it on and off after a delay of 10 seconds.
3. Implement the hardware and software for automatic street light logic.

21ECC32 Image Processing

3 0 2 4

Course Outcomes

1. Interpret fundamental concepts of digital images
2. Execute various conversion operations on digital images
3. Implement image enhancement techniques in spatial and frequency domain
4. Implement various filters for image restoration
5. Execute segmentation techniques for digital images
6. Assess various image compression techniques

COs – POs Mapping

COs	PO_1	PO_2	PO_4	PO_5	PSO_2
1	2	-	2	2	2
2	3	2	2	3	3
3	3	2	2	3	3
4	3	2	2	3	3
5	3	2	2	3	3
6	3	2	2	3	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Digital Image Fundamentals

Fundamental steps in digital image processing, Elements of visual perception, Image sampling and quantization, Basic relationships between pixels, Image types and formats: Binary image, Gray image, Color image, Color fundamentals, Color models: RGB, HSI and CMY.

Pseudo color Image Processing, Full Color Image Processing

Practical Components

1. Perform basic image operations viz., image read and write on binary image, gray image and color image.
2. Convert a color image to gray image and binary image.
3. Convert color image from RGB model to HSI and HSI to RGB.
4. Perform Image comparison using subtraction

12+8 Hours

Unit II

Image Enhancement

Enhancement in spatial domain: Histogram Processing, Smoothing, Sharpening,

Image transforms and its properties: 2D Discrete Fourier Transform, Discrete Cosine Transform, Discrete Wavelet Transform, Enhancement in Frequency Domain: Smoothing and Sharpening Filters.

Walsh Transform, Haar Transform

Practical Components

1. Carry out intensity transformations on image
2. Perform histogram equalization on digital image
3. Implement image smoothing/sharpening in spatial domain
4. Perform image smoothing/sharpening in frequency domain

12+8 Hours

Unit III

Image Restoration

Image Restoration model, Noise models, Restoration using spatial filtering, Periodic noise reduction by frequency domain filtering, Linear Position-Invariant Degradations, Inverse filtering, Minimum Mean Square Error Filtering, Constrained Least squares filtering.

Estimating the degradation function, Geometric Mean filter

Practical Components

1. Perform image restoration in spatial domain using restoration filters
2. Construct filters to remove various noise effects on the image (Uniform, Gaussian, Poisson, Salt & pepper)
3. Carry out frequency domain filtering for image restoration
4. Perform restoration using Inverse filtering

` **12+8 Hours**

Unit IV

Image Segmentation and Compression

Image segmentation: Fundamentals, Point, Line and Edge detection, Thresholding, Region based Segmentation,

Image Compression: Fundamentals, Image Compression Models, Lossless Compression: Huffman, Arithmetic, Run Length Encoding, Lossy Compression: Transform coding.

Watershed algorithm, JPEG compression standard

Practical Components

1. Implement Prewitt and Sobel operators on an image for edge detection
2. Perform image segmentation based on thresholding
3. Implement Huffman coding technique
4. Implement transform coding technique

12+8 Hours

Total: 48+32 Hours

Textbook (s)

1. Rafel C. Gonzalez and Richard E. Woods, Digital Image Processing, Pearson Education, 3rdEdition 2011
2. S. Sridhar, Digital Image Processing, Oxford publishers, 2nd Edition, 2016
3. Rafel C. Gonzalez and Richard E. Woods, Digital Image Processing using MATLAB, Gatesmark Publishing, 3rdEdition 2020

Reference (s)

1. S. Jayaraman, S. Esakirajan, T. Veerakaumar, Digital Image Processing, McGraw Hill publishers, 2011
2. Anil K. Jain, Fundamentals of Digital Image Processing, Pearson Education, 1st Edition, 2015
3. M. Sonka, V. Hlavac, R. Boyle, Image Processing, Analysis and Machine Vision, Vikas Publishing House, 2001

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1(%)	Int. Test 2 (%)	Lab Examination (%)
Remember	25	10	--
Understand	40	45	--
Apply	35	45	100
Analyse	--	--	--
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. List the 6 fundamental steps in digital image processing
2. Define image enhancement
3. Define image segmentation
4. State the lossy compression
5. List out the 3 color models

Understand

1. Interpret the process of image sampling and quantization
2. Summarize the fundamental steps in digital image processing
3. Represent RGB color model
4. Explain the properties of 2D Discrete Fourier Transform
5. Illustrate contrast stretching transformation function to increase the dynamic range of the gray levels in the image

Apply

1. Consider the image segment shown below. Compute N_4, N_8 distances

   3 1 2 1 (q)
   2 2 0 2
   1 2 1 1
   (p) 1 0 1 2

2. Compute histogram equalization for a given 8x8 image
3. Compute the efficiency of Huffman Coding for the given symbols

Symbol	a1	a2	a3	a4	a5	a6
Probability	0.1	0.4	0.06	0.1	0.04	0.3

4. Implement segmentation on given image using bimodal thresholding
5. Show that a linear, spatially –invariant degradation system with additive noise can be modeled in the spatial domain as the convolution of the degradation function with an image followed by addition of noise

21EC004 Virtual Instrumentation

3 0 2 4

Course Outcomes

1. Interpret basic building blocks of virtual instrumentation
2. Execute various graphical programming environment in virtual instrumentation
3. Asses various applications based on loops and error handling techniques
4. Execute various functions and I/O files
5. Implement Various applications on DAQ
6. Assess various real communications and interfacing

COs – POs Mapping

COs	PO_1	PO_2	PO_4	PO_5	PSO_2
1	2	-	2	2	2
2	3	2	2	3	3
3	3	2	2	3	3
4	3	2	2	3	3
5	3	2	2	3	3
6	3	2	2	3	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Introduction of LabVIEW and Basic Programming:

LabVIEW Environment, Parts of VI, Front panel designing and working environment, Definitions of Control and Indicators, Types of Control and Indicators, Explanations of Controls Palette, Explanations Block Diagram and its working, Terminals, Functional Platte, Status Bar or Window tool bar, How to use Numerical functions, Designing of Boolean operations, Comparator applications

Practical Components

1. Generate basic signals using LabVIEW.
2. Perform Boolean operations using LabVIEW
3. Design traffic lights in LabVIEW
4. Calculating the power and energy of a given signal in LabVIEW.

12+8 Hours

Unit II

Implementing a VI and Programming Loops

About For loops, How to use Shift registers, while loop designing, Flat Sequences, Applications based on Loops-Average Temperature VI, Temperature Multiplot VI, Square root VI, Arrays, Auto-Indexing of arrays, Array Functions and different array operations, Polymorphism and Polymorphic Vis, Clusters & Cluster Functions, creating cluster, bundle and unbundle operations on Cluster, Error Clusters to capture and merge errors while running a VI, String Functions for formatting and manipulating strings

Practical Components

1. Build a VI to generate random numbers between 0 and 1000 until it matches a number selected by user
2. Build a VI to measure the temperature and display the average last three temperatures
3. Build a VI to plot the temperature and the running average on the same chart
4. Build the VI to measure square root of a number

12+8 Hours

Unit III

File I/O and Customizing Vis

File I/O VIs and Functions, High-Level File I/O Vis , Low-Level File I/O VI and Functions , Formatting Spreadsheet Strings Configuring the Appearance of Front Panels, Opening Sub VI Front Panels when a VI Runs, Keyboard Shortcuts for Controls, Editing VI Properties, Customizing the Controls and Functions Palettes

Practical Components

1. Build a VI to store three arrays in the spreadsheet

2. Build a VI to log the current temperature into ASCII file.
3. Build a VI to extract specific data
4. Build a VI to extract specific field

` **12+8 Hours**

Unit IV

Data Acquisitions Process and Instrument Control based on Embedded Controllers:

MAX and VISA explanations, GPIB communications, Serial communications and interfacing methods, acquiring the real time digital data to the LabVIEW User interface, controlling the LED operations, Acquiring of real time analog sensor values, controlling the Motors.

Practical Components

1. Build a VI that measures the voltage signal of the DAQ
2. Build a VI that counts pulses from the quadrature encoder on the DAQ
3. Build a VI that converts the number of events generated by quadrature encode to digital number display on LED
4. Build a VI that communicates with a serial or GPIB interface to an instrument using VISA functions.

12+8 Hours
Total: 48+32 Hours

Textbook (s)

1. Gary W. Johnson, Richard Jennings, 'Lab-view Graphical Programming', McGraw Hill Professional Publishing, 2001.

2. Lisa K Wells, Lab view for Everyone||, Prentice Hall of India.

Reference (s)

1. Barry Paton, —Sensor, transducers and Lab view||, Prentice Hall of India 2000.
2. Buchanan, W. —Computer buses||, CRC Press 2000

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1(%)	Int. Test 2 (%)	Lab Examination (%)
Remember	25	10	--
Understand	40	45	--
Apply	35	45	100
Analyse	--	--	--
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. Draw and explain the graphical and VI models with design flow
2. Explain the essential need for Virtual Instrumentation and compare it with the traditional instruments.
3. Explain the role of different hardware's and software's in VI.

Understand

1. Explain the three parts of LabVIEW with three floating palette.
2. Discuss in detail about While and For Loops with Examples
3. Discuss in detail about different structures with examples
4. Describe in detail about various file types and File I/O functions

Apply

1. What are the NI-IMAQ and IMAQ vision functions used to acquire and display images?

2. Show the process how DAQ Assistant is used to acquire and generate signals with procedure for creating, configuring, Test and generate Lab VIEW code using DAQ Assistant.
3. Design a VI for pulse rate measuring in LabVIEW

21EC005 Cryptography and Network Security

3 0 2 4

Course Outcomes

1. Understand the fundamentals of cryptography, encryption and decryption algorithms
2. Understand the symmetric cryptographic algorithms
3. Explain the various asymmetric key cryptosystems and asymmetric key ciphers
4. Interpret the message authentication and integriry.
5. Demonstrtae the functionalities of Email, IP and Web security
6. Understand various system security vulnerabilities

CO–PO Mapping

CO	PO1	PO3	PO4	PO5	PSO1
1	3	3	1	1	3
2	3	3	1	2	3
3	1	2	3	2	1
4	3	1	1	2	3
5	1	3	3	2	1
6	1	3	2	1	1

3–Strongly linked | 2–Moderately linked | 1–Weakly linked

Unit I Introduction to Number theory and Classical Encryption techniques

Computer Security Concepts, A model for network security, Divisibilty and Division algorithm, Euclidean algorithm, Modular arithmetic, prime numbers, Fermat's and Euler theorem, Testing of primality, Chinese Remainder Theorem, Discreate logarithms. Symmetric Cipher Model, Substitution Techniques: Caeser, Playfair, Hill, Vernem ciphers. Transportation Techniques.

Practical Components

1. Write a program that contains a string (char pointer) with a value "Hello world". The program should AND or and XOR each character in this string with 127 and display the result.
2. Caesar Cipher Implementation
3. Vernem Cipher Implementation
4. Hill Cipher Implementation

12+8 Hours

Unit II Symmetric Key and Asymmetric Key Cryptosystems

Symmetric Key Cryptosystems: Principles of Private Key System, Data Encryption Standard (DES), Strength of DES. DES with double key, DES with triple key, **Finite fiels:** Polynomial arithmetic with coefficient in Zp, Finding GCD, Modular polynomial arithmetic, Finding multiplicative inverse.

Asymmetric key ciphers: RSA cryptosystem – Key distribution – Key management – Diffie Hellman key exchange -ElGamal cryptosystem – Elliptic curve arithmetic-Elliptic curve cryptography.

Practical Components

5. Simple D.E.S Implementation
6. DES with double key
7. R.S.A Implementation
8. Diffie–Hellman key exchange Implementation

12+8 Hours

Unit III

Message Authentication and Integrity

Authentication requirement – Authentication function – MAC – Hash function – Security of hash function and MAC – SHA –Digital signature and authentication protocols – DSS- Entity Authentication: Biometrics, Passwords, Challenge Response protocols- Authentication applications – Kerberos, X.509

Practical Components

9. ElGamal public key cryptosystem Implementation
10. Digital signature generation

11. Calculate the message digest of a text using the SHA-1 algorithm.
12. Generation of Hash function **12+8 Hours**

Unit IV

Security Practice and System Security

Electronic Mail security – PGP, S/MIME – IP security – Web Security – System Security: Intruders – Malicious software – viruses – Firewalls.

Practical Components

13. Using Snort identify the Intruders if any.
14. Find the Packet Information using short.
15. Write program to detect malicious viruses
16. Write a program to provide security Electronic Mails

12+8 Hours
Total: 48+32 Hours

Text Books:

1. William Stallings, "Cryptography And Network Security – Principles and Practices", 7th edition, Pearson Education Limited 2017.
2. Atul Kahate, "Cryptography and Network Security", 2nd edition, Tata McGraw-Hill, 2003.
3. Behourz A Forouzan, Cryptography and Network Security, 2nd edition, Tata McGraw-Hill, 2011.

Reference Books:

1. Matt Bishop ,"Computer Security art and science ", Second Edition, Pearson Education, 2002
2. Wade Trappe and Lawrence C. Washington, "Introduction to Cryptography with Coding Theory" Second Edition, Pearson Education, 2007
3. Jonathan Katz, and Yehuda Lindell, Introduction to Modern Cryptography, CRC Press, 2007
4. Douglas R. Stinson, "Cryptography Theory and Practice", Third Edition, Chapman & Hall/CRC, 2006
5. Wenbo Mao, "Modern Cryptography – Theory and Practice", Pearson Education, First Edition, 2006.
6. OWASP top ten security vulnerabilities: http://xml.coverpages.org/OWASPT opTen.pdf

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Lab Examination (%)
Remember	30	30	--
Understand	40	40	--
Apply	30	30	100
Analyze	--	--	--
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

SAMPLE QUESTION (S)

Remember

1. Mention any two security attacks
2. List any two goals of security.
3. Define Hash function.

Understand

1. Differentiate between asymmetric and symmetric key cryptography.
2. How do we achieve authentication?
3. Differentiate between the two applications of hash function.

Apply

1. How do we Apply PGP to the Email Security?
2. Implement firewall using iptables command.
3. Can message encryption itself provide measure of authentication?

21CS503 Computer Networks

3 0 2 4

Course Outcomes

1. Gain the knowledge of the basic Data Communication System and Computer Network Systems.
2. Classify various wired and wireless transmission media for data communication networks
3. Apply knowledge of different techniques of error detection and correction to detect and solve error bit during data transmission
4. Obtain the skills of subnetting, routing mechanisms and congestion issues in network design.
5. To be able to work with different network tools.
6. Understand the internal functionalities of main protocols such as HTTP, SNMP, TCP, UDP, IP

CO-PO Mapping

COs	PO1	PO2	PO4	PO5	PSO1	PSO2
1	2	1	2	2	2	2
2	*3*	2	2	3	*3*	*3*
3	3	2	2	3	3	3
4	2	-	2	3	2	2
5	1	-	2	3	1	1
6	2	-	2	3	2	2

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Introduction to Data Communications: Components, Data Representation, Data flow

Network hardware, Network software, OSI, TCP/IP Reference models, Example Networks: ARPANET, Internet.

Physical Layer: Transmission media: Guided media- twisted pairs, coaxial cable, fiber optics, unguided media-Wireless transmission, Switching Techniques: Circuit Switching-Packet Switching-Message Switching.

Taxonomy of networking devices

Practical Components:

1. a) Familiarization with Networking Components and devices: LAN Adapters - Hubs – Switches - Routers etc.
2. Familiarization with Transmission media and Tools: Co-axial cable - UTP Cable - Crimping Tool - Connectors etc.
3. Preparing the UTP cable for cross and direct connections using crimping tool.
4. a) To configure the IP address for a computer connected to LAN and to configure network parameters of a web browser for the same computer.
   b) Configuration of TCP/IP Protocols in Windows

12 + 8 Hours

Unit II

Design Issues: Framing-error detection and correction-CRC-Elementary Data link Protocols: Stop and wait-Sliding Window protocols: Go-back-n-Selective Repeat-Medium Access sub layer: Channel allocation methods-Multiple Access protocols: ALOHA-CSMA-IEEE Standard 802.3 and Ethernet-

Data Link Control Protocols: HDLC-SLIP-PPP

Practical Components:

5. Implement the data link layer framing methods:
   a) Character stuffing method
   b) Bit Stuffing method
6. Implement on a data set of characters the two CRC polynomials: CRC 12 - CRC 16
7. Develop a simple data link layer that performs the flow control using
   a) The sliding window protocol,
   b) Go-Back-N Protocol.

12 + 6 Hours

Unit III

Network Layer: Design issues, Routing algorithms: shortest path routing, distance vector routing, Flooding, Hierarchical routing, Broadcast, Multicast, Congestion Control Algorithms-Approaches to Congestion Control, Quality of Service- leaky bucket algorithm, token bucket algorithm, The Network

layer in the internet-IPv4 Protocol, IP Addresses, Subnetting.

Internet control protocols

Practical Components:

8. Implement Dijkstra's algorithm to compute the Shortest path through a graph.

9. Take an example subnet graph with weights indicating delay between nodes. Now Obtain Routing table art each node using distance vector routing algorithm.
10. Take an example subnet of hosts. Obtain broadcast tree for it.
11. Write a program for congestion control using Leaky bucket algorithm.

12 + 8 Hours

Unit IV

Transport Layer: Transport Services, Elements of Transport protocols, Connection management, TCP and UDP protocols. Application Layer –Domain name system, SNMP, Electronic Mail, World Wide Web, HTTP

Proxy Servers, Data compression

Practical Components:

12. a) Installing of internal modem and connecting to Internet.
    b) To configure WiFi for your PC.
13. Wireshark
    a) Packet Capture Using Wire shark
    b) Starting Wire shark
    c) Viewing Captured Traffic
    d) Analysis and Statistics & Filters.
14. Do the following using NS3 Simulator
    a) NS3 Simulator-Introduction and installation
    b) Simulate to Find the Number of Packets Dropped
    c) Simulate to Find the Number of Packets Dropped by TCP/UDP
    d) Simulate to Find the Number of Packets Dropped due to Congestion
    e) Simulate to Compare Data Rate& Throughput.
    f) Simulate to Plot Congestion for Different Source/Destination
    g) Simulate to Determine the Performance with respect to Transmission of Packets
15. Write a program for how to connect and transfer data between two nodes with each other.
16. Study and build a sample network topology to configure it for dynamic routing protocol using NS3

12 + 10 Hours
Total: 48+32 Hours

Textbook (s)

1. Andrew S Tanenbaum, Computer Networks, 5th Edition, Pearson Education /PHI, 2013
2. Behrouz A. Forouzan, Data Communications and Networking, 5thEdition, Tata McGraw Hill Higher Education, 2013

Reference (s)

1. Willam Stallings, Data and Computer Communications,8th Edition, Pearson Prentice Hall, 2007
2. W.A. Shay, Thomson, Understanding communications and Networks, 3 rd Edition, Cengage Learning, 2005

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Lab Examination (%)
Remember	22	10	--
Understand	35	30	--
Apply	20	20	100
Analyze	20	20	--
Evaluate	--	20	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. List the applications of Computer Networks
2. Write two differences between OSI and TCP/IP models.
3. State 5 key assumptions in Dynamic channel allocation?
4. State the purpose of DNS.
5. Define congestion.

Understand

1. Illustrate OSI Reference model.
2. Explain various design issues of data link layer.
3. What are the responsibilities of Data Link layer and explain Pure Aloha and Slotted Aloha protocols.
4. Describe Distance Vector routing algorithm with example and explain count to infinity problem 5. Represent the Manchester encoding for the bit stream: 0001110101.

Apply

1. What is the check summed frame transmitted if the message is 1101011011 and the generator polynomial is x 4 + x + 1 using CRC
2. Can you think of any circumstances under which an open-loop protocol, (e.g., a Hamming code) might be preferable to the feedback-type protocols.
3. Assuming that all routers and hosts are working properly and that all software in both is free of all errors, is there any chance, however small, that a packet will be delivered to the wrong destination?

Analyze

1. The following data fragment occurs in the middle of a data stream for which the byte-stuffing algorithm described in the text is used: A B ESC C ESC FLAG FLAG D. What is the output after stuffing?
2. The following character encoding is used in a data link protocol: A: 01000111; B: 11100011; FLAG: 01111110; ESC: 11100000 Show the bit sequence transmitted (in binary) for the four-character frame: A B ESC FLAG when each of the following framing methods are used: (a) Character count. (b) Flag bytes with byte stuffing. (c) Starting and ending flag bytes, with bit stuffing.
3. Analyze Data link protocols almost always put the CRC in a trailer rather than in a header.

Evaluate

1. Consider the user of differentiated services with expedited forwarding. Is there a guarantee that expedited packets experience a shorter delay than regular packets? Justify

21EC603 Digital Signal Processing Lab

0 0 3 1.5

Course Outcomes

1. Demonstrate various DSP operations.
2. Compute linear, circular convolution and FFT of a signal
3. Compare IIR and FIR filter design Techniques
4. Execute different type of multi rate signal processing techniques
5. Implementation of discrete computations and digital filters using DSP processor
6. Outline the process of noise reduction in real time signals

COs	PO_1	PO_2	PO_4	PO_5	PSO_2
1	2	-	2	3	2
2	3	2	2	3	3
3	3	2	2	3	3
4	3	2	2	3	3
5	3	2	2	3	3
6	3	3	2	3	3

List of Experiments
Students will perform minimum twelve Experiments
Implement the following using MATLAB

1. Generation of Discrete time signals and sum of sinusoidal signals
2. Determination of power and power spectral density of the given sequence
3. Verification of Linear convolution of two given sequences with different lengths.
4. Verification of circular convolution of two given sequences with different lengths.
5. To find frequency response of a given system(transfer function/ difference equation)
6. To find DFT / IDFT of given DT signal.
7. Determination of FFT for a given sequence.
8. Implementation of LP IIR filters for a given sequence.
9. Implementation of HP IIR filters for a given sequence.
10. Implementation of LP FIR filters for a given sequence.
11. Implementation of HP FIR filters for a given sequence.
12. Implementation of Decimation Process
13. Implementation of Interpolation Process
14. Implementation of I/D sampling rate converter
15. Generation of DTMF signals.
16. Impulse Response of First Order and Second Order Systems.

Implement the following using TMS processor

17. To study the architecture of DSP chips – TMS 320C 6X Instructions
18. linear convolution of two given sequences and plot
19. Perform MAC operation using various addressing modes
20. Generation of various signals and random noise
21. Magnitude response FIR LP filter using rectangular windowing technique
22. Magnitude response IIR LP filter

List of Augmented Experiments[1]

1. Mixing and separation of two voice signals
2. Add noise above 3kHz and then remove the Interference for Audio signal
3. Design a notch filter for the removal of power line interference from ECG signal by using TMS processor

Reading Material(s)

1. Digital Signal Processing by Sanjit K.Mitra 2nd Edition , TATA McGraw Hill
2. Digital Signal Processing, Principles, Algorithms, and Applications: John G. Proakis, Dimitris G. Manolakis, Pearson Education / PHI, 2007.
3. Digital signal processing lab Manual

21MPX01 Mini Project

0 0 3 1.5

Course Outcomes

1. Identify a contemporary engineering application to serve the society at large
2. Use engineering concepts and computational tools to get the desired solution
3. Justify the assembled/fabricated/developed products intended
4. Organize documents and present the project report articulating the applications of the concepts and ideas coherently
5. Demonstrate ethical and professional attributes during the project implementation
6. Execute the project in a collaborative environment

COs – POs Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
1	3	2				3	2						3	3
2	3	3			3								3	3
3	3	3	3	2							2		3	3
4										3		2	3	3
5								3					3	3
6									3				3	3

3–Strongly linked | 2–Moderately linked | 1–Weakly linked

21ESX02 Employability Skills II

0 0 2 2

Course Outcomes

1. Demonstrate oral communication and writing skills as an individual to present ideas coherently
2. Develop life skills with behavioral etiquettes and personal grooming.
3. Assess analytical and aptitude skills.
4. Develop algorithms for engineering applications.
5. Solve engineering problems using software.
6. Utilize simulation tools for testing.

COs – POs Mapping

COs	PO1	PO2	PO5	PO8	PO10	PO12
1					3	2
2				1	2	2
3	2	1		2		
4	2		2			
5	2		2			
6	2		2			

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

1. Communication Skills, Confidence and Quantitative Aptitude

Resume (Recap): Resume? Templates? Mistakes to be avoided in a Resume and Steps to be followed in preparing it.

Group Discussions (Recap) & Practice: GD? Stages of a GD, Skills assessed in a GD, Blunders to be avoided, How to excel in a GD?

Practice sessions and sharing Feedback. (Screening sample Videos)

Interview Skills: Interview? Types of Interview, Dos & Don'ts, Skills assessed in an Interview, Mistakes to be avoided, How to equip oneself to excel? How to handle the Typical Interview Questions? (with Examples)

Mock Interviews: Practice sessions with Feedback.

Exercises related to Communication: Email Writing, Voice Versant., etc.

7Hours

2. Quantitative Aptitude

Time and Distance, Problems on Trains, Blood relations, Ratio and Proportions, Calendars, Clocks

8 Hours

Unit II

Verilog constructs for building the testbench

Procedural, Continuous and Procedural continuous assignments, Verilog parameters, inter assignment delay, intra assignment delay, Stem tasks: display tasks, tasks for file operation; Combinational UDPs and Sequential UDPs

Practical Components

1. Perform the simulation of a Verilog testbench to demonstrate the Procedural continuous assignments.
2. Perform the simulation of a Verilog testbench to demonstrate the Verilog parameters.
3. Perform the simulation of a Verilog testbench to demonstrate the inter assignment delay
4. Perform the simulation of a Verilog testbench to demonstrate the inter assignment delay
5. Develop a Verilog testbench that displays the content of a given file
6. Develop a Verilog testbench that writes the content into the file
7. Develop a Verilog testbench to display the file content and detect the end of a given file
8. Perform the simulation of a Verilog testbench to demonstrate the combinational UDP.
9. Perform the simulation of a Verilog testbench to demonstrate the sequential UDP

15 Hours

Total Hours 30

Textbook (s)

2. Padmanabhan, Tattamangalam R., and B. Bala Tripura Sundari. Design Through Verilog HDL. John Wiley & Sons, 2003.

Reference (s)

3. Palnitkar, Samir. *Verilog HDL: a guide to digital design and synthesis*. Vol. 1. Prentice Hall Professional, 2003.
4. Ciletti, Michael D. *Advanced digital design with the Verilog HDL*. Vol. 1. Upper Saddle River: Prentice hall, 2003.

21HSX12 CC & EC Activities II

0 0 1 1

Course Outcomes

1. Interpret and present the abstractive technical information through an activity
2. Think critically in providing solutions to the generic and common problems
3. Demonstrate the creative thinking in dealing with liberal arts
4. Instill team sprit through active engagement with the peer
5. Develop programs of common interest having social impact
6. Empower the under privileged through motivational activities

COs – POs Mapping

COs	PO6	PO7	PO9	PO10
1	-	-	-	3
2	3	2	-	-
3	3	-	-	-
4	-	-	3	-
5	3	-	-	-
6	3	-	-	-

20BEA01 Environmental Studies

0 0 0 0

Course Outcomes:

1. Translate the learner's attitude to think globally and act locally
2. Motivate environmental organizations to create a concern about our present state of Environment.
3. Find solutions for conservation of natural resources
4. Identify the benefits of ecosystem conservation, biodiversity protection, implement pollution prevention and control measures
5. Illustrate social issues of environmental protection and adopt sustainable developmental practices
6. Perceives the basic structure of environmental policy and law pertaining to specific environmental issues (water quality, air quality, biodiversity protection, Forest, etc.)

COs – POs Mapping

COs	PO_1	PO_6	PO_7	PO_{12}
1	1	2	3	1
2	2	-	3	2
3	3	3	-	2
4	-	2	3	2
5	-	-	3	1
6	-	3	2	1

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Multidisciplinary Nature of Environmental Studies & Natural Resources

Definition, Scope and Importance, Multidisciplinary nature of Environmental Studies, Value of Nature - Productive, Aesthetic/Recreation, Option, Need for Public Awareness, Institutions (BNHS, BVIEER, ZSI, BSI) and People in Environment (Medha Patkar, Sundarlal Bahuguna, Indira Gandhi, Rachael Carson).
Natural Resources: Renewable and Non-renewable resources – Importance, uses, overexploitation/threats, and conservation of (i) forest (ii) water (iii) mineral (iv)food and (v) energy resources. (The topics include benefits and problems associated with dams, mining and case studies), role of an individual in conservation of natural resources.

Unit II
Ecosystem & Biodiversity
Ecosystems: Concept of an ecosystem, Structure and function of an ecosystem, Biogeological cycles (Energy flow, Carbon and Nitrogen Cycles), Ecological succession, Food chains, food webs and ecological pyramids. Introduction, types, characteristic features, structures and functions of the following ecosystems: a. Forest Ecosystem b. Aquatic Ecosystem
Biodiversity and its Conservation: Definition and levels of biodiversity, Bio-geographical classification of India, hot spots of biodiversity - India as a mega diversity nation, Threats to biodiversity, Endangered and endemic species of India, Conservation of biodiversity: In-situ and Ex-situ conservation.

Unit III
Environmental Pollution & Social Issues
Environmental Pollution: Definition, Cause, effects, control measures and case studies of: Air pollution b. Water pollution c. Soil pollution
Solid waste Management: Causes, effects and control measures of urban and industrial wastes. Disaster management (floods and cyclones)
Social Issues and the Environment: Sustainability, Urban problems related to energy, Water conservation and watershed management, Resettlement and rehabilitation of people; Environmental ethics: Issues and possible solutions, global warming, ozone layer depletion, Consumerism and waste products

Unit IV
Human Population and the Environmental Acts
Human Population and the Environment: Population growth, Affluence, Technology and Environmental Impact (Master Equation), Population explosion and Family Welfare Programme, Value Education, HIV/AIDS, Women and Child Welfare, Role of information Technology in Environment and human health.
Environment Protection Acts: Air (Prevention and Control of Pollution) Act, Water (Prevention and control of Pollution) Act, Wildlife Protection Act and Forest Conservation Act. Issues involved in enforcement of environmental legislation.

Text Book(s) and Reading Material (s)

1. T. E. Graedel, B. R. Allenby, Industrial Ecology and Sustainable Engineering, 1st Edition, Pearson Publications, 2009.
2. W. P. Cunningham, M.A. Cunningham, Principles of Environmental Science, 6th Edition, Tata McGraw Hill, 2008.
3. A. Kaushik, C. P. Kaushik, Perspectives in Environmental Studies, 4th Edition, New Age International Publishers, 2008.
4. T. E. Graedel, B. R. Allenby, Industrial Ecology and Sustainable Engineering, 1st Edition, Pearson Publications, 2009.
5. E. Bharucha, Textbook of Environmental Studies, 1st Edition, University Press (India) Pvt. Ltd., 2005.
6. H. S. Peavy, D. R. Rowe, G. Tchobanoglous, Environmental Engineering, 1st Edition, McGraw Hill Int. ed., 1984.
7. http://172.30.1.222/wbc/it/schedule.aspx.
8. http://172.30.1.8/wbc/it/coursepage.aspx.
9. https://www.edx.org/course/environmental-protection-and-sustainability.

21ECC13 Analog and Mixed Signal VLSI Design

3 0 0 3

Course Outcomes

1. Illustrate the MOS device models Single-stage amplifiers and Current mirrors
2. Explain the operation of Differential amplifiers
3. Demonstrate the operation of Op-amp internal circuits
4. Demonstrate the operation of switched capacitor circuits
5. Demonstrate the operation of continuous and discrete-time filters
6. Outline the operation of data conversion circuits

COs – POs Mapping

COs	PO1	PO2	PO3	PSO1
1	2	-	-	2
2	2	-	-	2
3	3	2	2	3
4	3	2	2	3
5	3	2	2	3
6	3	2	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Basic Analog Circuits

Introduction analog design, MOS device capacitances, MOS Small-signal model, Second order effects, CS amplifier with resistive load, CS stage with current source load, CS stage with source degeneration, Cascode stage, Current Mirrors: Basic current mirrors, small-signal analysis of a simple current source, Common source amplifier with current mirror as a load, Cascode current mirrors

Advanced MOS Modelling, Single Stage Amplifiers

11 Hours

Unit II

Differential amplifiers and Op-amp circuit

Differential amplifiers: single-ended and differential amplifier operation, basic differential pair, differential pair with MOS loads, differential pair with current source load, Operational Amplifiers: One stage Op-Amp: Simple Op-Amp topologies, Cascode Op-Amp, Folded cascode op-amp, Two-stage Op-Amp, comparison of op-amp topologies, slew-rate

Common Mode Feedback, Power supply rejection

13 Hours

Unit III

Switched capacitors and filters

Switched capacitors: Introduction to the switched capacitor circuits, non-idealities in switched-capacitor filters, Basic building blocks, parasitic sensitive integrator, parasitic insensitive integrator, Filters: First order switched capacitor filter and its analysis, switch sharing, fully differential first-order switched capacitor filter, charge injection

Switched-capacitor filter applications, Stability of Discrete-Time Filters

13 Hours

Unit IV

Data converters

Basics of data converters; Analog to Digital converters: Algorithmic, Two-step, Folding, Pipeline, Interpolating ADCs; Thermal code converters, Hybrid DACs, Bandgap reference

Time-interleaved A/D converters, Binary-array charge-redistribution D/A converter

11 Hours

Total: 48 Hours

Textbook (s)

1. Behzad Razavi, Design of Analog CMOS Integrated Circuits, 2nd Edition, McGraw-Hill, 2017
2. Tony Chan Carusone, David Johns, Kenneth Martin: Analog Integrated Circuit Design, 2nd Edition, John Wiley Publications, 2011
3. R. Jacob Baker, CMOS mixed-signal circuit design, Wiley India, IEEE press, reprint 2008
4. Rudy V. dePlassche, CMOS Integrated ADCs and DACs, Springer, Indian edition, 2005

Reference (s)

1. Philip E. Allen & Douglas R. Holberg, CMOS Analog Circuit Design, Oxford University Press, 2002
2. M. Burns et al., An introduction to mixed-signal IC test and measurement by, Oxford university press, first Indian edition, 2008
3. R. Jacob Baker, CMOS circuit design, layout and simulation, Revised second edition, IEEE press, 2008
4. Arthur B. Williams, Electronic Filter Design Handbook, McGraw-Hill, 1981
5. R. Schauman, Design of analog filters, Prentice-Hall, 1990
6. Ramakant A. Gayakwad, Op-Amps and Linear Integrated Circuits, Fourth edition, Pearson Education, 2015

SAMPLE QUESTION (S)
Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Examination (%)
Remember			--
Understand	70	25	--
Apply	30	75	50
Analyse	--		50
Evaluate	--	--	
Create	--	--	--
Total (%)	100	100	100

Remember

1. Recall the analog signal processing.
2. Recall the discrete-time signal processing
3. Reproduce the sampling theory
4. Reproduce the basic differential pair
5. List any two-analog continuous-time filters
6. Recall the basics of analog discrete-time filters.

Understand

1. Explain the single-ended differential amplifier circuit.
2. Abstract the second-order effects in MOS FET.
3. Explain the basic differential amplifier
4. Illustrate the MOS models
5. Illustrate the MOS modeling

Apply

1. Construct a cascode current mirror using CMOS
2. Demonstrate the non-idealities in switched capacitor circuits
3. Demonstrate high output impedance current mirrors
4. Demonstrate the applications of switched capacitor filter.
5. Demonstrate a simple CMOS current mirror circuit. **[Open-Book Question]**

Analyze

1. Outline the circuit for Successive approximation ADCs.
2. Outline the circuit for Dual slope ADCs.
3. Organize the Flash ADCs.
4. Outline a Pipeline ADC circuit.
5. Organize the High-resolution DACs**[Open-Book Question]**

21ECC23 Real Time Operating Systems

3 0 0 3

Course Outcomes

1. Summarize a real time system
2. Exemplify modelling of time constraints
3. Assess General Purpose Operating System and Real Time Operating System
4. Explain real time communication
5. Compare various Real Time Scheduling Approaches
6. Organize different real time operating systems

COs – POs Mapping

COs	PO1	PO2	PSO1
1	2		2
2	2		2
3	3	2	3
4	2		2
5	3	2	3
6	3	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Real Time System

Introduction to real time system, applications of a real time system, characteristics of real time systems, safety and reliability, Types of real time tasks – Hard real time task, Soft real time task and Firm real time task , timing constraints, classification of timing constraints – delay constraint, deadline constraint and duration constraint, modeling timing constraints.

fault Tolerant Applications, classification of systems on the basis of real time task

12 Hours

Unit II

Real Time Operating System

Operating system Basics, features of General Purpose Operating System (GPOS), features of Real Time Operating System (RTOS), Process, Threads and Tasks, multiprocessing and multitasking, types of multitasking, Task synchronisation – Racing and Deadlock. Task synchronisation techniques – Mutual Exclusion through busy waiting/spin lock, Mutual Exclusion through sleep & Wakeup, selection criteria for an RTOS

Identify some RTOS for review, Embedded Programming in C

12Hours

Unit III

Real Time Scheduling Approaches

Task scheduling, Non-Preemptive Scheduling – First-Come-First-Served (FCFS) scheduling, Last-Come-First-Served (LCFS) scheduling, Shortest Job First (SJF) scheduling, Priority Based scheduling. Preemptive Scheduling – Preemptive Shortest Job First (SJF) scheduling/Shortest Remaining Time (SRT), Round Robin (RR) Scheduling. Rate monotonic algorithm (RMA)

Rate Monotonic Algorithm, Hybrid scheduler

13 Hours

Unit IV

Commercial Real Time Operating Systems

Unix as a real time operating system, Windows as a real time operating system, POSIX

Real time Communication - Basic concepts, Real-time communication in a LAN and Real-time communication over packet switched networks, applications requiring real time communication

µC/OS-II, VxWorks

11 Hours

Total: 48 Hours

Textbook (s)

1. Rajib Mall, Real-time Systems Theory and Practice, 1st edition, Pearson Publication, 2008

2. Shibu .K.V, Introduction to Embedded Systems, 1st Ed, Tata McGraw Hill Education Private Limited, 2009.

Reference (s)

1. Jane W. S. Liu, Real-Time Systems, Pearson Education, 2000.
2. C.M. Krishna and K.G. Shin, Real-Time Systems, TMH, 2009.

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Examination (%)
Remember			--
Understand	70	40	--
Apply	30	50	50
Analyze	--	10	50
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. Define real-time system.
2. List few applications of real-time systems.
3. What is meant by fail safe state?
4. Name any two important sensor devices and two actuators used in real time systems.

Understand

1. Explain the basic model of real-time system.
2. Explain characteristics of real-time systems.
3. Explain the key differences between the characteristics of a soft-real time task such as web browsingand a non-real time task such as e-mail delivery.

Apply

1. In a real time system what is the difference between a performance constraint and a behavioral constraint? Give practical examples of each type of constraint.
2. Draw a schematic model showing the important components of a typical hard real system. Explain the working of output interface using a suitable schematic diagram. Explain using a suitable circuitdiagram how analog to digital conversion is achieved in an output interface.
3. Draw a schematic model showing the important components of a typical hard real system. Explain the working of input interface using a suitable schematic diagram. Explain using a suitable circuit diagram how digital to analog conversion is achieved in an input interface.
4. What are the benefits of modelling timing constraint? Identify and model the type of time constraint in the following statement by using extended finite state machine (EFSM):

i. "Once 1st digit has been dialled on the telephone handset, the next digit must be dialled with in next seconds"

ii. "Once dial tone appear the 1st digit must be pressed on the telephone handset within 30 seconds otherwise system will go to idle state and idle tone produced" **[Open-Book Question]**

Analyze

1. What do you mean by task instance? Distinguish between relative dead line and absolute deadline. Identify the constraints that a set of periodic real-time tasks need to satisfy for RMA to be optimalscheduler for the set of tasks?
2. Three processes P1, P2 and P3 with estimated completion time 10ms, 5ms and 7ms respectively enter the ready queue together in the order P1, P2, P3. Calculate the waiting time and turn around time for each process and the average waiting time and average turn around time for the

followings:

i. 'First-Come-First-Served' Non-preemptive scheduling**[Open-Book Question]**
ii. 'Shortest job first' Non-preemptive scheduling
iii. Assume that there is no I/O waiting for the process

21ECC33 Multimedia Communications

3 0 0 3

Course Outcomes

1. Summarise basics of different multimedia networks and applications.
2. Demonstrate compression techniques of text and audio.
3. Assess video compression techniques.
4. Illustrate different multimedia information networks.
5. Demonstrate enterprise networks and Internet.
6. Justify the real-time entertainment networks and high speed modems.

COs – POs Mapping

COs	PO1	PO2	PSO2
1	2		2
2	2		2
3	3	2	3
4	2		2
5	3	2	3
6	3	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Introduction

Introduction, Multimedia information representation, multimedia networks, multimedia applications, Networking terminology, Digitization principles, Text, Images, Audio and Video.

Application QoS, Video content

12 Hours

Unit II

Data Compression

Introduction, Compression principles, Text compression techniques, Image Compression techniques, Audio compression techniques, Video compression techniques.

JPEG Decoding, Reversible VLCs

12 Hours

Unit III

Multimedia Information Networks

Introduction, LANs, Ethernet/IEEE802.3, Token ring, Bridges, FDDI, High-speed LANs, LAN protocol, IP Datagrams, Fragmentation, IP Address, ARP and RARP, Routing algorithms, ICMP, Support, IPv6.

Multisite LAN Interconnection technologies, QoS Support

12 Hours

Unit IV

Networks and Modems: Introduction, Cell format, Switch and Protocol Architecture ATM LANs, Cable TV Networks, Satellite Television Networks, Terrestrial television networks, ISDN, DSL and Cable Modems

ATM MANs, High Speed PSTN Access Technologies.

12 Hours

Total: 48 Hours

Textbook (s)

1. Fred Halsall, Multimedia Communication, Pearson education, 2001.
2. K. R. Rao, Zoran S. Bojkovic and Dragorad A. Milovanovic, Multimedia Communication Systems, Pearson education, 2004.

Reference (s)

1. Ralf Steinmetz, Klara Nahrstedt, Multimedia: Computing, Communications and Applications, Pearson education, 2004.
2. John Billamil, Louis Molina, Multimedia: An Introduction, PHI, 2002.
3. Nalin K. Sharda, Multimedia Information Networking, PHI, 2003.
4. Prabhat K. Andleigh, Kiran Thakrar, Multimedia Systems Design, PHI, 2004.

SAMPLE QUESTION (S)
Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Examination (%)
Remember			
Understand	50	30	
Apply	50	60	50
Analyse	--	10	50
Evaluate	--	--	
Create	--	--	
Total (%)	100	100	100

Remember

1. Define Multimedia information representation.
2. List few applications of multimedia.
3. Why is data compression necessary for Multimedia?
4. What is MIDI? How is a basic MIDI message structured?

Understand

1. Briefly explain how the LZW Transform Operates. What common compression methods utilize this transform?
2. What two levels of functionality are to be considered when multimedia systems are to be designed? Briefly define these levels.
3. For each common multimedia data type discuss what common functionalities should be supported by a multimedia system.

Apply

1. Suppose we want to encode the Oxford Concise English dictionary which contains about 159,000 entries. Can you transmit each word as an 18-bit number?
2. It is required to produce a Multimedia mail system. What media should be supported in such a mail system and how should an application facilitate assembly, delivery and reading of the mail.
3. Briefly explain why we need to have less than 24-bit colour representations and why this is sometimes a problem. Give examples where 8-bit colour representation have an advantage in terms of image/video processing? **[Open-Book Question]**

Analyze

1. How can MIDI be used with modern data compression techniques? Briefly describe how such compression techniques may be implemented?
2. Compare the main facilities that must be provides in a system designed to support the integration of multimedia into a multimedia presentation??
3. Suppose there are 24 bits per pixel available for a colour image. Humans are more sensitive the red and green than to blue, by a factor of approximately 1.5 times. How may we design a simple colour representation to make use of the bits available? **[Open-Book Question]**

21EC006 Wireless Sensor Networks

3 0 0 3

Course Outcomes

1. Exemplify wired and wireless networks for real time applications
2. Summarize sensor network architectures for various applications
3. Interpret various operations in sensor node and transceiver design
4. Classify suitable medium access protocols, routing protocols, security protocols and radio hardware
5. Implement prototype sensor networks using commercial components
6. Differentiate various infrastructure management and sensor network platform tools

COs – POs Mapping

COs	PO_1	PO_2	PSO_1	PSO_2
1	2		2	2
2	2		2	2
3	2		2	2
4	2		2	2
5	3	2	3	3
6	3	2	3	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit- I

Sensor Network architectures

Introduction to ISO/OSI layers, Key definitions of WSN, Advantages of sensor networks, Unique constraints and challenges, Driving Applications, Enabling Technologies for WSNs. Single node architecture-Hardware Components, Energy consumption of sensor nodes, Operating system and execution environment, Network architecture-Sensor network scenarios. Optimization goals, Figures of merits, Gate way concepts.

Smart sensors, SoC sensor nodes **12 hours**

Unit-II

PHY and MAC Layer Protocols

Physical layer, Transceiver design considerations, Personal area Networks (PANs), Hidden Node and Exposed node Problem, Topologies of PANs, Topologies of MANETs, and Topologies of WANETs. Issues in designing a MAC protocol for WSNs, Design goals of a MAC protocol for WSNs, Classification of MAC Protocols, and Contention based protocols.

Network throughput, Network lifetime **12 Hours**

Unit- III

Network and Transport Layer Protocols

Issues in designing a routing protocol for ad-hoc wireless networks, Classification of routing Protocols, Table-driven routing protocols, On-demand routing protocols, Hybrid routing Protocols, Routing Protocols with efficient flooding mechanism, Hierarchical routing protocols , Power aware routing Protocols, Proactive routing. Issues in designing Transport layer for ad-hoc wireless Networks, Design goals of Transport layer for ad-hoc wireless Networks, Classification of transport layer solutions, TCP over ad-hoc wireless networks.

Lifetime of sensor nodes, IP based sensor networks **12 Hours**

Unit IV

Application Layer and programming challenges

Topology control, Clustering, Time Synchronization, Localization, Positioning, Sensor Tasking and Control, Security in ad-hoc wireless networks, Network security requirements, Issues and Challenges in security provisioning, Network security attacks, Key management, Security Routing in ad-hoc wireless networks. Sensor node hardware-Berkeley motes, Programming challenges, Node level software platforms, Node level simulators, State centric programming.

WSN in IoT, WSN for Health monitoring **12 Hours**

Total: 48 Hours

Textbook (s)

1. C. Siva Ram Murthy and B.S.Manoj, Ad Hoc Wireless Networks: Architectures and Protocols, PHI, 2004.

2. Jagannathan Sarangapani, Wireless Ad- hoc and Sensor Networks: Protocols. Performance and Control , CRC Press,2007
3. Holger Karl &Andreas Willig, Protocols and Architectures for Wireless Sensor Networks, John Wiley, 2005.

Reference (s)

1. KazernSohraby, Daniel Minoli, &TaiebZnati, Wireless Sensor Networks- Technology, Protocols and Applications John Wiley, 2007.
2. Feng Zhao & Leonidas J. Guibas, Wireless Sensor Networks- An Information Processing Approach, Elsevier, 2007.
3. C.K. Toh , Ad- Hoc Mobile Wireless Networks: Protocols & Systems, Prentice Hall, 2002
4. C. S. Raghavendra, Krishna M. Sivalingam, Wireless Sensor Networks, Springer, Ist Edition,2006
5. S Anandamurugan ,Wireless Sensor Networks, Lakshmi Publications, 2010

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Examination (%)
Remember	45	--	--
Understand	45	50	--
Apply	10	50	50
Analyse	--	--	50
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. State the transceiver design considerations
2. List out any two different types optimization goals
3. Define wireless sensor network
4. Recall the design goals of Transport layer protocol

Understand

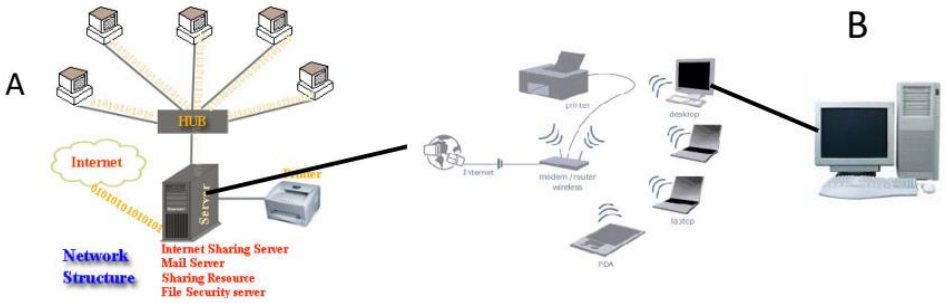
1. Explain the hidden node and exposed node problem
2. Summarize issues in designing MAC protocol for ad-hoc wireless networks
3. Illustrate the unique constraints and challenges of WSNs

Apply

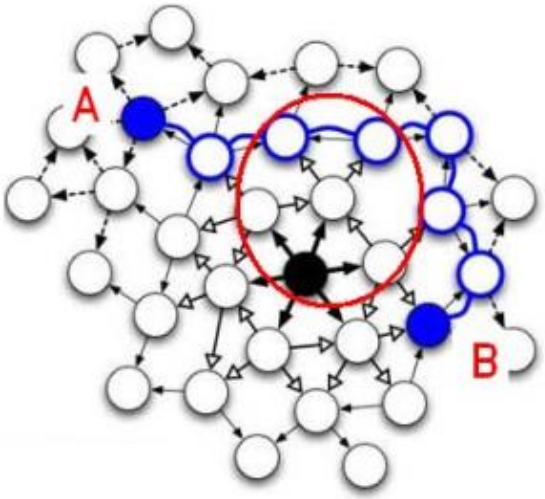
1. Implement different Network security attacks
2. Demonstrate the programming challenges and applications of WSN
3. Construct different transport layer solutions for any real time application **[Open-Book Question]**

Analyse

1. Compare and Contrast between connection based MAC protocols with Scheduling mechanism
2. Organize different ways of designing a Routing protocols for Ad Hoc Wireless networks
3. Outline the unique constraints and challenges of WSNs
4. Compare between active and passive attacks
5. For the following scenario, please suggest a good Transport Layer strategy to take care of packet loss issues. Source: A; Destination: B. The left side is a campus cable based network. The right side is a wireless, multi-hop network. Provide clear solution. **[Open-Book Question]**



6.Suppose we have a network as follows. The marked part is a network congestion area. If A wants to send packets to B, how does A detect such a congestion area? Suggest a reasonable, low-overhead solution.



21IT403 Operating Systems

3 0 0 3

Course Outcomes

1. Understand computer resources and operating system management.
2. Analyze various CPU Scheduling Algorithms for Process Management.
3. Examine process synchronization and coordination of operating system.
4. Analyze the Main Memory Management and allocation strategies.
5. Identify the use of Virtual Memory management policies with respect to storage management.
6. Identify the need of File-System Interface and I/O Systems.

CO – PO Mapping

COs	PO_1	PO_{12}
1	3	2
2	3	2
3	3	2
4	3	2
5	3	2
6	3	1

3–Strongly linked | 2–Moderately linked | 1–Weakly linked

Unit I

Operating-Systems Overview and Process Management

Operating-System Overview: Computer-System Organization and Architecture, Operating-System Structure, Operating-System Operations & Services, System Calls & its types.
Threads: Multi Core Programming, Multithreading Models, Thread Scheduling algorithms.
Process Management: Process Concepts, Process Scheduling Criteria, Scheduling Algorithms and evaluation.
Thread issues, Multilevel Queue, Multilevel feedback Queue Scheduling

12 Hours

Unit II

Inter Process Communication Mechanism

Process Synchronization: Cooperative process, the Critical Section Problem, Peterson's Solution, Synchronization Hardware, Semaphores, Classical Synchronization problems, Monitors.
Deadlocks: Deadlock Characterization, Methods for Handling Deadlocks, Deadlock Prevention, Deadlock Avoidance & Detection, Recovery from Deadlock.
Synchronization Examples-Synchronization in Solaris, Synchronization in Linux. **12 Hours**

Unit III

Memory Management

Main Memory: Contiguous Memory allocation, Swapping, Segmentation, Paging, Segmented paging, Multilevel paging.
Virtual Memory Management: Demand Paging, Page Replacement algorithms, Allocation of Frames.
Structure of page table, Thrashing, Memory-Mapped Files **12 Hours**

Unit IV

File System Interface & I/O Systems

Mass-Storage Structure: Disk structure, Disk Scheduling, Disk management, Raid Structure.
File System: Access Methods, Directory Structures, Allocation Methods, Free-Space Management.
I/O Systems: I/O hardware Application of I/O Interface, Kernel I/O Sub-System.
File Sharing, File System Recovery **12 Hours**

Total: 48 Hours

Textbook (s)

1. Abraham Silberschatz, Greg Gagne, Peter B. Galvin, Operating System Concepts, 9th Edition, Wiley, 2016.
2. Harvey M. Deitel, Paul J. Deitel, David R. Choffnes, Operating Systems, 3rd Edition, Pearson Prentice Hall, 2004.

Reference (s)

1. William Stallings, Operating Systems: Internals and Design Principles, 7th Edition, Pearson Prentice Hall, 2013.
2. D. M. Dhamdhere, Operating systems: A Concept based Approach, 2nd Edition, TMH, 2006.
3. Crowley, Operating System: A Design Approach, 1st Edition, TMH, 2001.
4. Andrew S Tanenbaum, Modern Operating Systems, 3rd Edition, PHI, 2009.

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Examination (%)
Remember	20	20	--
Understand	40	30	--
Apply	30	30	50
Analyze	10	20	50
Evaluate			
Create	--	--	--
Total (%)	100	100	100

Remember

1. List any four operating systems
2. Define operating system
3. List four operating system services

Understand

1. Explain System calls
2. Explain the role memory management in operating system
3. Illustrate the working principle critical section problem

Apply

1. When multiple transactions are being executed by the operating system in a multiprogramming environment, there are possibilities that instructions of one transaction are interleaved with some other transaction. Apply the suitable concept to overcome the problem
2. Give an example of a scenario that might benefit from a file system supporting an append-only access write.

Analyze

1. Context switching between two threads of execution within the operating system is usually performed by a small assembly language function. In general terms, what does this small function do internally?
2. Compare CPU scheduling algorithms
3. Analyze the general strategy behind deadlock prevention and give an example of a practical deadlock prevention method.

Open Book Exam Questions

1. A file to be shared among different processes, each of which has a unique number. The file can be accessed simultaneously by several processes, subject to the following constraint: the sum of all unique numbers associated with all processes currently accessing the file must be less than n. Write a monitor to co-ordinate the access to the file. Ou may want to write start_access and end_access monitor procedures.

2. Consider a paging system with the page table stored in memory:
    a. If a memory reference takes 200 nanoseconds, how long does a paged memory reference take?
    b. If we add associative registers, and 75% of all page-table references are found in the associative registers, what is the effective memory reference time?

21CS603 Software Engineering

3 0 0 3

Course Outcomes

1. Explain the need of Software Life Cycle Models
2. Build end-user requirements into system and software requirements,
3. Summarize the system models of software engineering
4. Identify and apply appropriate software architectures and patterns to carry out high level design
5. Choose various testing techniques during software development
6. Categorize Risk management and Software quality for software products

CO–PO Mapping

CO	PO4	PO5	PO8	PO11	PSO1
1	3	3	2	2	2
2	3	3	2	2	2
3	3	2	2	2	2
4	2	2	2	2	2
5	2	3	2	2	2
6	2	3	2	2	2

3–Strongly linked | 2–Moderately linked | 1–Weakly linked

UNIT – I

Introduction to Software Engineering and SDLC, Software Myths, CMMI, Process models: Linear Sequential model, Prototyping model, Evolutionary models: Spiral model, Agile developmental methodologies-Scrum & XP

Incremental model, software development : Product based and application based **12 Hours**

Unit II

Software Requirements: Functional and non-functional requirements, user requirements, system requirements, interface specification.

Software Requirements Engineering Process, Feasibility studies, Requirement's elicitation and analysis, requirements validation.

System models: Context models, behavioural models, data models, object models. \

Structure of Software Requirements Document, Structured analysis methods **12 Hours**

Unit III

Design concepts: Data design, software architecture, Architectural styles and patterns, User interface design - Golden rules, User interface analysis and design and steps. Conceptual model of UML, basic structural modeling, Sattic and Dynamic UML diagrams : class diagrams, sequence diagrams, collaboration diagrams, use case diagrams, etc.,

Data Acquisition System - Monitoring and Control System **12 Hours**

Unit IV

Testing strategies and Risk Management: Testing levels: Unit testing, integration testing, system testing – alpha and beta testing, Testing Types: black box and white box testing techniques, Cyclomatic Complexity, debugging, Risk management - Risk types, strategies, estimation and Planning. Software Quality - Quality assurance and its techniques

Software measurement, metrics for software quality **12 Hours**

Total: 48 Hours

Textbook (s)

1. Roger S. Pressman, Software Engineering, A Practitioner's Approach, 8th Edition, McGraw-Hill International Edition, 2015
2. I. Sommerville, Software Engineering, 7th Edition, Pearson education, 2004.

3. Rajib Mall, Fundamentals of software Engineering, 4th Edition, Eastern Economy Edition, 2014.

Reference(s)

1. K K Aggarwal and Yogesh Singh, Software Engineering,3rd Edition, New age international publication,2008

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Examination (%)
Remember	30	30	--
Understand	40	40	--
Apply	30	30	50
Analyze	--	--	50
Evaluate	--	--	--
Create	--	--	
Total (%)	100	100	100

Remember

1. Define software engineering.
2. List different types software myths.

Understand

1. Describe software architecture styles and patterns .
2. Illustrate golden rules for user interface design.

Apply

1. Applying the process of requirement analysis, discuss how the requirements can be collected for a project.
2. Applying debugging strategy fin an error from a code?

Analyze

1. Compare and Contrast software life cycle models.

2. Analyze risk types in the risk management.

Open Book Exam Questions

Assume that 10 errors have been introduced in the requirements model and that each error will be amplified by a factor of 2:1 into design and an addition 20 design errors are introduced and then amplified 1.5:1 into code where an additional 30 errors are introduced. Assume further that all unit testing will find 30 percent of all errors, integration will fi nd 30 percent of the remaining errors, and validation tests will fi nd 50 percent of the remaining errors. No reviews are conducted. How many errors will be released to the field.

21EC007 Design for Testability

3 0 0 3

Course Outcomes

1. Identify various types of faults in digital circuits
2. Interpret the concepts of test generation for digital circuits
3. Implement testable digital logic circuits
4. Interpret system level DFT approaches
5. Explain self test algorithms
6. Outline self checking design

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PSO_1
1	2	-	-	2
2	2	-	-	2
3	3	2	1	3
4	2	-	-	2
5	2	-	-	2
6	3	2	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Testing and fault modeling

Introduction to testing, Faults in Digital Circuits, Modeling of faults Logical Fault Models, Fault detection and redundancy, Fault equivalence, Fault Location, Fault dominance, Struck at faults, multiple struck at faults, Logic simulation, Types of simulation, Delay models.

Gate level event driven simulation, Ambiguous delay

12 Hours

Unit II

Test pattern generation

Test generation for combinational logic circuits**:** Fault oriented ATG, Fault Independent ATG, Random test generation based on non-uniform distributions. Test generation for sequential circuits**:** TG using iterative array model, Simulation based TG, TG using RTL models, Random test generation for sequential cicuits.

ATG systems, TG methods

12 Hours

Unit III

Design for testability

Testability Concepts, Ad-hoc based design: Test points, monostable-multivibrators, logical redundancy. Generic scan based design: Full serial integrated scan, non-serial scan. Classical scan based design.

Built-In Self-Test: BIST concepts, hardcore, levels of test. Test pattern generation for BIST**:** Exhaustive testing, Pseudo random testing, Pseudo exhaustive testing, Constant weight patterns. BIST Architectures: BEST, RTS, LOCST, Automatic Test Equipment(ATE)",Memory built in self-Test (MBIST) and Logic Built_in _Test(LBIST)

CSTP, BILBO

12 Hours

Unit IV

Fault diagnosis

Logical Level Diagnosis**:** Basic concepts, fault dictionary, Guided probe testing, Diagnosis by UUT reduction, Fault Diagnosis for Combinational Circuits. Self-checking design: Basic concepts, Error detecting and error correcting codes, multiple bit errors, self-checking circuits, Parity check function, Self-checking for equality checkers.

Self-checking for m/n checkers, Berger code

12 Hours

Total: 48 Hours

Textbook (s)

1. M.Abramovici, M.A.Breuer and A.D. Friedman, Digital systems and Testable Design, Jaico Publishing House, 2000.
2. P.K. Lala, Digital Circuit Testing and Testability, Academic Press, 1997.

Reference (s)

1. M.L.Bushnell and V.D.Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Kluwer Academic Publishers, 2000.
2. A.L.Crouch, Design Test for Digital IC's and Embedded Core Systems, Prentice Hall International, 2002.

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Examination (%)
Remember	20	20	--
Understand	50	40	--
Apply	30	40	70
Analyse	--	--	30
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. List out the different types of simulation.
2. List out the different types self test and test algorithms
3. Define gate level event driven simulation
4. Define testability
5. List out the different fault models

Understand

1. Interpret the various operations of a test algorithm.
2. Explain principle involved in the fault modeling
3. Illustrate the working principle of fault detection
4. Compare controllability and observability
5. List out the different fault models
6. Explain system level DFT approaches

Apply

1. Carryout DFT approaches and with the help of neat sketch write the working of each level.
2. Demonstrate the application of MBIST circuits
3. Find delay models and with a neat sketch write the working of each model.
4. Demonstrate the application of generic scan based design
5. List out the different fault models
6. Derive a functional testing model.
7. Generate embedded core testing model.
8. Consider the circuit of figure 1. Let f be the fault b SA0 and g be a SA1.
9. Does f mask g under the test 0110? Does f mask g under the test 0111?

Are the faults f and {f,g} distinguishable?

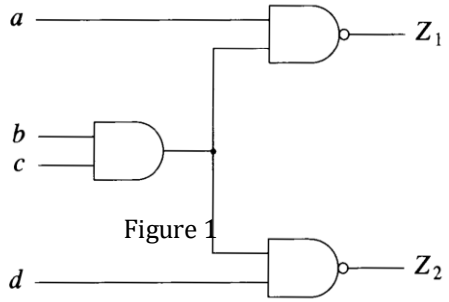


Figure 1

Analyse

.

1. Compare and Contrast between classical scan based design and generic scan based design.
2. Is increasing the efficiency of test pattern generation for BIST? If yes, Justify
3. Compare and Contrast between specific and generic offline BIST architectures.
4. Demonstrate the application of generic scan based design
5. Defend Simultaneous Self Test (SST)?
6. Use only implications to show that the fault f s-a-0 in the circuit of figure 2 is undetectable.

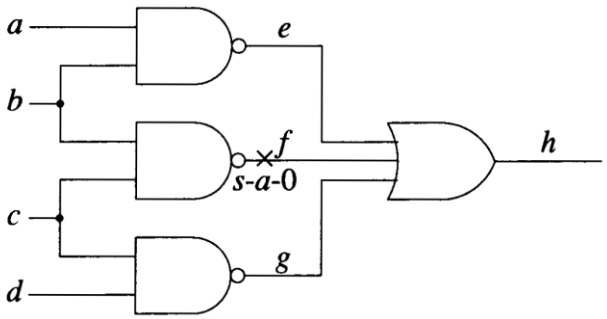


Figure 2

21EC008 Biomedical Signal Processing

3 0 0 3

Course Outcomes

1. Illustrate the waveform characteristics of biomedical signals
2. Explain the properties of biomedical signals
3. Assess algorithms for cardiological signal processing
4. Demonstrate suitable algorithms for neurological signal processing
5. Outline the diagnosis of biomedical signals
6. Explain the different adaptive algorithms for noise and interference cancellations

COs–POsMapping

COs	PO1	PO2	PSO2
1	2	-	2
2	2	-	2
3	3	2	3
4	3	2	3
5	3	2	3
6	2	-	2

3–Stronglylinked|2–Moderatelylinked|1–Weakly linked

Unit I

Introduction to Biomedical Signals

Introduction to biomedical signals The nature of biomedical signals, action potential, objectives of biomedical signal analysis, Difficulties in biomedical signal analysis, computer aided diagnosis, Basic electrocardiography, the brain and its potentials, the electrophysiological origin of brain waves, EEG signals and its characteristics, EEG analysis. Basic EMG.

Electroneurogram, Phono cardiogram

12 Hours

Unit II

Cardiological Signal Processing

Basic ECG, Electrical Activity of the heart, ECG data acquisition, ECG lead system, ECG parameters & their estimation, Use of multiscale analysis for ECG parameters estimation, Noise & Artifacts, arrhythmia analysis monitoring, long-term continuous ECG recording, direct ECG data compression techniques.

Cardiotocography, Methods of Monitoring Fetal Heart Rate.

12 Hours

Unit III

Neurological Signal Processing

Basic EEG, Linear prediction theory, the autoregressive method, spectral error measure, adaptive segmentation, Sleep EEG: data acquisition and classification of sleep stages, the markov model and markov chains, template matching for EEG-spike-and-wave detection.

Dynamics of sleep-wake transitions, Hypnogram model parameters

12Hours

Unit IV

Adaptive Interference/Noise Cancellation

The wiener filtering problem, principle of an adaptive filter, the Widrow Hoff least mean square adaptive algorithm, Adaptive noise canceller: cancellation of 50/60hz interference in ECG, cancelling donor heart interference in heart-transplant ECG, cancellation of high frequency noise in electro-surgery.

X-Ray imaging, Magnetic Resonance Imaging, CT scan **12 Hours**

Total:48 Hours

Text Book (s) :

1. D.C.Reddy, Biomedical Signal Processing: Principles and Technique's Tata McGraw Hill, 2005.
2. E.N. Bruce, Biomedical Signal Processing and Signal Modelling, John Wiley and Sons, 2007.

3. MetinAkay, Biomedical Signal Processing, Academic Press, 2012.

References:

1. Sörnmo,Bioelectrical Signal Processing in Cardiac & Neurological Applications, Academic Press,2005.
2. Rangayyan,Biomedical Signal Analysis,Wiley 2002.
3. I Enderle, Introduction to Biomedical Engineering, Elsevier, 2nd Edition, 2005

SAMPLEQUESTION(S)

InternalAssessmentPattern

CognitiveLevel	Int.Test1 (%)	Int.Test2 (%)	Open Book Examination (%)
Remember	35	30	--
Understand	35	35	--
Apply	30	35	60
Analyze	-		40
Evaluate	--	--	--
Create	--	--	--
Total(%)	100	100	100

Remember

1. Define Systole and diastole
2. Define BioElectrode
3. List out the requirements for Bio amplifier
4. List out the biomedical signals

Understand

1. Explain about cardio vascular system
2. Explain how the Imaging Techniques is helpful in biomedical signal processing
3. Illustrate the classification of EEG rhythms based on the frequency bands
4. Compare the biomedical signal of ECG, EEG, and EMG
5. Explain the application of MRI with neat diagram

Apply

1. Implement an algorithm to detect QRS complexes in an ongoing ECG signal
2. Show that a signal averaging improves the signal to noise ratio by a factor of square root of M
3. Design an adaptive filter using LMS algorithm
4. Construct an optimal filter to remove noise from a signal, given that the signal and noise processes are independent, stationary, random processes**[Open Book Examination Questions]**
5. Demonstrate a typical ECG waveform over one cardiac cycle indicating the important component waves, and the typical intervals between them. Label each wave or interval with the corresponding cardiac event or activity. **[Open Book Examination Questions]**

Analyze

1. Organize the spectral estimation in biomedical signals**[Open Book Examination Questions]**
2. Compare normal segmentation and adaptive segmentation**[Open Book Examination Questions]**

21EC009 UHF and EHF communication systems

3 0 0 3

Course Outcomes

1. Interpret the various subsystems and their parameters
2. Asses various multiple access techniques and spread spectrum techniques
3. Demonstrate the concepts of Link Design
4. Explain RADAR parameters and applications
5. Demonstrate the operation of CW and MTI RADARs
6. Differentiate the tracking techniques for RADARs

COs – POs Mapping

COs	PO1	PO 2	PSO2
1	2	-	2
2	2	-	2
3	3	2	3
4	2	-	2
5	3	2	3
6	3	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Introduction to Satellite and Subsystems

Introduction to spectrum characteristics and Spectrum ranges, basic Concepts of Satellite Communications, Applications, Orbital Mechanics, Orbit determination, Look Angle determination, Orbital perturbations, launches and launch vehicles, Orbital effects in communication systems performance. Attitude and orbit control system, telemetry, tracking, Command and monitoring, power systems, communication subsystems, Satellite antennas.

Orbit Determination, Manned Space Vehicles

12 Hours

Unit II

Satellite Link Design and Multiple Access Techniques

Satellite link Design: Basic transmission theory, system noise temperature and G/T ratio.

Multiple Access Techniques: Frequency Division Multiple Access (FDMA), Time Division Multiple Access (TDMA), Demand Assignment Multiple Access (DAMA) , Code Division Multiple Access (CDMA), Spread spectrum techniques

Design of UP & Down links, Packet radio systems and Protocols

12 Hours

Unit III

Basics of Radar

Introduction, Maximum Unambiguous Range, Radar Block Diagram and Operation, Simple form of Radar Equation, Radar Cross Section of simple Targets, PRF and Range Ambiguities. CW and Frequency Modulated Radar: Doppler Effect, CW Radar-Block Diagram, MTI and Pulse Doppler Radar**:** Introduction, Principle, Delay Line Cancellers, Filter Characteristics, Blind Speeds, Double Cancellation, Staggered PRFs, Range Gated Doppler Filters, MTI versus Pulse Doppler Radar.

Multiple Frequency CW Radar, MTI Radar with Power Oscillator Transmitter **13 Hours**

Unit IV

Tracking Radar

Tracking with Radar, Sequential Lobing, Conical Scan, Amplitude Comparison monopulse radar using one coordinate system and Phase Comparison methods, Target Reflection Characteristics and Angular Accuracy, Tracking in Range, Acquisition and Scanning Patterns, Comparison of Trackers, Radomes, Frequency scan Arrays, Radar Display types, Branch type and Balanced type duplexers

Amplitude Comparison using two coordinate system, Circulators as Duplexers

11 Hours

Total: 48 Hours

Textbook (s)

1. Timothy Pratt, Charles Bostian and Jeremy Allnutt, WSE, Satellite Communications, Wiley Publications, 2nd Edition, 2004
2. Wilbur L. Pritchard, Robert A Nelson and Henri G.Suyderhoud, Satellite Communications Engineering, 2nd Edition, Pearson Publications, 2012
3. Merrill I. Skolnik Introduction to Radar Systems, Tata McGraw-Hill, Third Edition, 2001

Reference (s)

1. K.N. Raja Rao, Fundamentals of Satellite Communications, PHI, 2004
2. Dennis Roddy , Satellite Communications, McGraw Hill, 2nd Edition, 1996
3. Gottapu Sasibhushana rao, Microwave & Radar Engineering, Pearson Education, 2013

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Examination (%)
Remember		20	--
Understand	40	40	--
Apply	60	40	50
Analyze	--		50
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. List out some communication satellites with their RF bandwidths
2. List out any two advantages and disadvantages of satellite communication over other types ofcommunication methods
3. Define sub satellite point
4. Recall the salient features of transmit-receive (T/R) Earth station
5. Recall the merits and demerits of satellite communication
6. Define blind speed
7. Define a false alarm
8. State the purpose of duplexer

Understand

1. Illustrate the main functions of INSAT series of satellites
2. Explain the various orbital perturbations and possible remedial measures to overcome them
3. Explain the launching process of a geo stationary satellite with aid of diagram.
4. Compare spin stabilization and momentum stabilization
5. Explain the significance of space link equation
6. Explain the need for integration of radar pulses and how does this factor affect the radar range equation
7. Illustrate the importance of a CW radar with non-zero IF receiver with block diagram

Apply

1. Find the i)path eccentricity ii) orbital time period for a satellite whose apogee height is 4000 km andperigee height is 1000 km. Assume radius of earth 6370km
2. Assess that three communication GEO satellites are sufficient to provide coverage for the globe
3. Find the gain in dB for a 3m paraboloidal antenna operating at frequency of 12 GHz. Assume apertureefficiency of 0.55
4. A satellite at 12GHz operates with transmit power of 6W and antenna gain of 48.2 dBW. Find [EIRP]in dBW
5. Antenna has noise temperature of 35Kelvin and is matched to a receiver that has noise temperature of100Kelvin. Find i) Noise power density. ii) Noise power for 36 MHz bandwidth
6. Compute the expression for the impulse response characteristics of a matched filter receiver that maximizesthe peak-signal-to-noise-power ratio
7. Demonstrate range and Doppler measurements of the target using triangular FMCW radar with neatdiagrams.

Analyse

1. Compare and Contrast between geo stationary and non-geostationary orbits
2. Analyze atmospheric drag and earth's shape that cause orbital disturbances
3. Differentiate elevation and azimuth angles
4. Organize the link power budget equation and analyze the terms
5. Compare active and passive attitude control of satellites
6. Outline the range and Doppler measurements using FM-CW radar if the target is approaching the radar andexplain it for triangular frequency modulation with neat diagram
7. Differentiate MTI and pulse Doppler radar

OPEN Book

1. It is necessary to maintain False-Alarm-Rate as constant. Justify the statement
2. Differentiate tracking radar and search radar
3. Outline the tracking procedure using amplitude-comparison monopulse radar (one angular coordinate) andhow it is different from that of either sequential lobing or conical scan technique

21EC010 Neural Networks and Deep Learning

3 0 0 3

Course Outcomes

1. Illustrate the basic principles of neural networks fundamentals
2. Asses artificial neural networks and their learning strategy
3. Demonstrate the principles of single layer and multilayer feed forward neural networks and back Propagation algorithm
4. Classify various learning techniques
5. Demonstrate the architectures of CNN and RNN
6. Differentiate between machine learning, deep learning and artificial intelligence

COs – POs Mapping

COs	PO_1	PO_2	PSO_1	PSO_2
1	2	-	2	2
2	2	-	2	2
3	2	-	2	2
4	3	2	3	3
5	3	2	3	3
6	3	3	3	3

3– Strongly 2– Moderately 1– Weakly

Unit I

Introduction to Neural Networks

Introduction, structure and working of Biological Neural Network , Artificial Neuron Models ,Trends in Computing Comparison of BNN and ANN Characteristics of ANN, McCulloch -Pitts Model, Artificial Neuron Model, Operations of Artificial Neuron, Types of Neuron Activation Function, Classification Taxonomy of ANN-Connectivity, Neural Dynamics: Activation and Synaptic, Learning Strategy: Supervised, Unsupervised, Reinforcement, Learning Process: Error Correction Learning, Memory Based Learning, Hebbian Learning, Competitive, Boltzmann Learning.

Applications of Memory Based Learning **12 Hours**

Unit II

Single & Multilayer Feed Forward Neural networks

Perception Models: Discrete, Continuous and Multi -Category, Training Algorithms: Discrete and Continuous Perception Networks, Perception Convergence theorem, Limitations of the Perception Model, Credit Assignment Problem, Generalized Delta Rule, Gradient Descent, Back propagation neural network, Back Propagation Algorithm XOR Problem, Heuristics, Output Representation and Decision Rule, Feature Detection

Applications of BPNN **12 Hours**

Unit III

Leaning Algorithms

Supervised learning :Linear Regression, Logistic Regression, K Nearest Neighbour (KNN), Random Forest, Support Vector Machines (SVM), Un supervised learning: k-means, c-means, Apriori, Reinforcement learning: Q-Learning, Case Study

Risk Evaluation, Anomaly Detection **13Hours**

Unit IV

Convolutional Neural Networks and Recurrent Neural Networks

Introduction to CNNs, Convolution, Correlation, Filtering, Kernel filter, Principles behind CNNs, Multiple Filters, CNN architectures, Detection and Segmentation, Visualizing and Understanding, Advanced CNNs for computer vision, Introduction to RNNs, Unfolded RNNs

RNN applications, CNN applications **11 Hours**

Total: 48 Hours

Textbook (s)

1. James A Freeman and Davis Skapura, Neural Networks, Pearson Education, 2002.
2. Simon Haykin, Neural Networks-Acomprehensive foundation, Pearson Education, 2001
3. Bengio, Yoshua, Ian J. Goodfellow, and Aaron Courville. "Deep learning." An MIT Press

book in preparation. (2015).

Reference (s)

1. S. N. Sivanandam, S. Sumathi, S. N. Deepa, Neural Networks using MATLAB 6.0, TMH, 2006
2. B Yegnanarayana, Artificial neural networks, Prentice Hall of India, 1stEdition, 2005.

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Examination (%)
Remember			--
Understand	40	30	--
Apply	60	50	50
Analyze	--	20	50
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. Define NN
2. Define Axon
3. Define activation functions.
4. Define Chromosome
5. List two methods in which the information flows in a nervous system
6. List five unsupervised learning algorithms

Understand

1. Explain about the McCulloch-Pitts Model.
2. Explain about ANN
3. Explain about Learning Strategy
4. Explain the role of activation function in exhibiting the output from a neuron
5. Construct the 5 node pattern {0,1,1,0,1} by Hopfield network and explain the procedure for recalling andstoring
6. Explain Adaptive Resonance Theory and its type
7. Explain CPN and illustrate the steps involved in training algorithm of full CPN

Apply

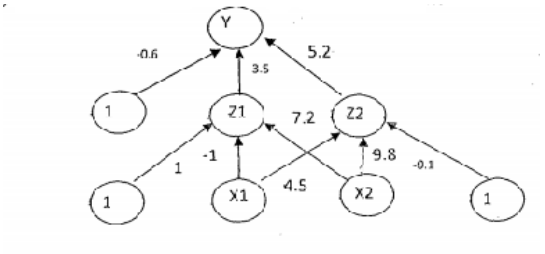
1. Construct a ANN circuit which makes the flow of data using multilayered and multilevel networks
2. Apply clusters of various datasets maintained by learning approach considering live example
3. Draw the neat architecture of hamming network and trace the inhibitory and excitatory neurons byconsidering an inconsistent vector

Analyse

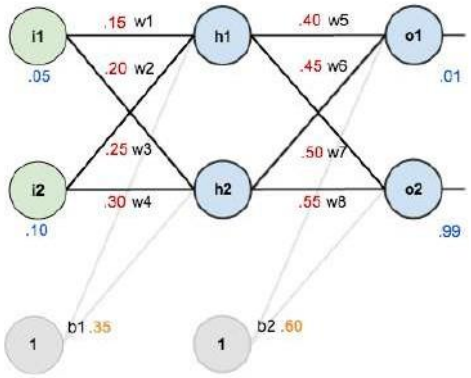
1. Differentiate between learning and training algorithms considering multilayer perceptron network and tracethe different types of networks obtained.
2. Differentiate between Counter Propagation Network and Adaptive Resonance Theory
3. Determine the energy function of continuous Hopfield network.
4. Determine a neural network that illustrates and learns how to balance an inverted pendulum.

Open Book Exam

1. Generate a neural net using BPNN algorithm for XOR logic functions. The architecture and the valuesof initial weights and biases are shown below.



2. Evaluate using Back Propagation algorithm for the below map considering weights , inputs and outputs



21PWX01Project Work

0 0 16 8

Course Outcomes

1. Identify a contemporary engineering application to serve the society at large
2. Use engineering concepts and computational tools to get the desired solution
3. Justify the assembled/fabricated/developed products intended
4. Organize documents and present the project report articulating the applications of the concepts and ideas coherently
5. Demonstrate ethical and professional attributes during the project implementation
6. Execute the project in a collaborative environment

COs – POs Mapping

COs	PO1	PO2	PO3	PO4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
1	3	2				3	2						3	3
2	3	3			3								3	3
3	3	3	3	2							2		3	3
4										3		2	3	3
5								3					3	3
6									3				3	3

3–Strongly linked | 2–Moderately linked | 1–Weakly linked

21SIX02 Summer Internship II

0 0 0 1.5

Course Outcomes

1. Demonstrate communication skills to meet the requirement of industry
2. Develop logical thinking and analytical skills to thrive in competitive examinations
3. Use mathematical concepts to solve technical quizzes
4. Develop technical skills to work out real time problems
5. Develop algorithms for different applications
6. Solve industry defined problems using appropriate programming skills

COs – POs Mapping

COs	PO_1	PO_2	PO_5	PO_6	PO_{10}	PO_{12}
1					3	
2	3	1				
3	3					
4	3	1	3			2
5	3	1	3	3		1
6	3	1	3			1

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

21EC012 Real-Time Systems Design and Analysis

0 0 0 3

Course Outcomes

1. Summarize a real time system
2. Exemplify hardware considerations of real time system
3. Assess the software design activities
4. Explain various engineering metrics considerations
5. Compare the performance analysis of various parameters during system design
6. Organize different performance optimization techniques

COs – POs Mapping

COs	PO1	PO2	PSO1
1	2		2
2	2		2
3	3	2	3
4	2		2
5	3	2	3
6	3	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Real Time Concepts and Hardware Considerations

Terminology, Real-Time System Design Issues, Example Real-Time Systems, Basic Architecture, Hardware Interfacing, Central Processing Unit, Memory, Input/Output, Enhancing Performance, Other Special Devices.

Brief History of real time systems, Flynn's Taxonomy for Parallelism

12 Hours

Unit II

Software System Design

Software Requirements Engineering - Requirements-Engineering process, Types of Requirements, Requirements Specification for Real-Time Systems, Formal Methods in Software Specification, Structured Analysis and Design, Software System Design - Properties of Software, Basic Software Engineering Principles, The Design Activity, Procedural-Oriented Design, Object-Oriented Design

Case Study in Software Requirements Specification for Four-Way Traffic Intersection Traffic Light Controller

12 Hours

Unit III

Performance Analysis and Optimization

Theoretical Preliminaries, Performance Analysis, Application of Queuing Theory, I/O Performance, Performance Optimization, Results from Compiler Optimization, Analysis of Memory Requirements, Reducing Memory Utilization.

Results from Compiler Optimization - Loop Unrolling and Loop Jamming

12 Hours

Unit IV

Engineering Considerations

Metrics, Faults, Failures, and Bugs, Fault-Tolerance, Systems Integration, Refactoring Real-Time Code, Cost Estimation Using COCOMO

Fault-Tolerance - The Kalman Filter, Refactoring Real-Time Code - Telltale Comments

12 Hours

Total: 48 Hours

Textbook (s)

1. Phillip A. Laplante, Real-time Systems Design and Analysis, 3rd edition, A JOHN WILEY & SONS, INC., PUBLICATION, 2004

Reference (s)

1. Jane W. S. Liu, Real-Time Systems, Pearson Education, 2000.

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Examination (%)
Remember			--
Understand	70	40	--
Apply	30	50	50
Analyze	--	10	50
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. Define real-time system.
2. List few examples of real-time systems.
3. What is meant by fail safe state?

Understand

1. Explain the fetch and execute cycles.
2. Illustrate the programmable logic array device.
3. Illustrate the programmable array logic device.

Apply

1. Demonstrate the use of finite state machine in system design.
2. Demonstrate the Response-Time Modeling.
3. Assess the Short-Circuiting Boolean Code. **[Open Book Examination]**

Analyze

1. Differentiate between state charts and perti nets.
2. Organize the analysis of Polled Loops.
3. Outline the Response-Time Analysis for Fixed-Period Systems. **[Open Book Examination]**

21EC013 Image Processing for Engineering Applications

0 0 0 3

Course Outcomes:

1. Illustrate the fundamentals of image processing using MATLAB
2. Summarize various Feature extraction techniques.
3. Asses spatial filters for image processing applications
4. Illustrate the concepts of image Registration
5. Illustrate the concepts of image fusion
6. Outline 3D image visualization

COs – POs Mapping

COs	PO_1	PO_2	PSO_2
1	2	1	2
2	2	1	2
3	3	2	3
4	2	1	2
5	2	1	2
6	3	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

IMAGE PROCESSING WITH MATLAB

What are Digital Images, Working with Image Data, Representing Images in MATLAB, Working with Image Data, Image Display vs. Image Data, Viewing Meta-Data and Images, Grayscale Images, Introduction to Color Spaces, Thresholding color Image, Adjusting Contrast in Grayscale and color Images, Other Approaches to Image Enhancement

12 Hours

Unit II

FEATURE EXTRACTION

First and second order edge detection operators, Phase congruency, Localized feature extraction - detecting image curvature, shape features, Hough transform, shape skeletonization, Boundary descriptors, Moments, Texture descriptors Autocorrelation, Co-occurrence features, Runlength features, Fractal model based features, Gabor filter, wavelet features.

12 Hours

Unit III

REGISTRATION AND IMAGE FUSION

Registration - Pre-processing, Feature selection - points, lines, regions and templates Feature correspondence - Point pattern matching, Line matching, Region matching, Template matching. Transformation functions - Similarity transformation and Affine Transformation. Resampling – Nearest Neighbour and Cubic Splines. Image Fusion - Overview of image fusion, pixel fusion, and wavelet based fusion -region based fusion.

12 Hours

Unit IV

3D IMAGE VISUALIZATION

Sources of 3D Data sets, Slicing the Data set, Arbitrary section planes, The use of color, Volumetric display, Stereo Viewing, Ray tracing, Reflection, Surfaces, Multiple connected surfaces, Image processing in 3D, Measurements on 3D images.

12 Hours

Total: 48 Hours

Text Book(s):

1. Ardeshir Goshtasby, " 2D and 3D Image registration for Medical, Remote Sensing and Industrial Applications",John Wiley and Sons,2005.
2. Anil K. Jain, Fundamentals of Digital Image Processing', Pearson Education, Inc., 2002.
3. John C.Russ, "The Image Processing Handbook", CRC Press,2007.

Reference Book(s)

1. Mark Nixon, Alberto Aguado, "Feature Extraction and Image Processing", Academic Press,2008.
2. Rafael C. Gonzalez, Richard E. Woods, Digital Image Processing', Pearson,Education, Inc.,Second Edition, 2004.
3. Rick S.Blum, Zheng Liu, "Multisensor image fusion and its Applications", Taylor& Francis,2006

SAMPLE QUESTION (S)
Internal Assessment Pattern

Cognitive Level	Int. Test 1	Int. Test 2 (%)	Open Book Examination (%)
Remember	25	20	--
Understand	40	45	--
Apply	35	35	50
Analyse	--	--	50
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember
1. Define image enhancement
2. List out the 3 color models
3. Represent RGB color model

Understand
1. Interpret the process of first and second order edge detection operators
2. Summarize the fundamental steps in Fractal model based features
3. Explain the Sources of 3D Data sets

Apply
1. Asses the Overview of image fusion in various apllications
2. Demonstrate the importance of Gabor filter and wavelet features in Image processing applications**[OPEN BOOK QUESTIONS]**

Analyse
1. Differentiate between image registration and image fusion in terms of processing and applications
2. Compare wavelet based fusion -region based fusion methods in terms of entropy, applications and transforms used**[OPEN BOOK QUESTIONS]**

21EC014 Computer Architecture

0 0 0 3

Course Outcomes

1. Summarize microarchitectures
2. Exemplify modelling of memory technologies
3. Assess base and bound registers
4. Compare various multithreading Approaches
5. Organize different multiprocessors
6. Explain network routing

COs – POs Mapping

COs	PO1	PO2	PSO1
1	2		2
2	2		2
3	3	2	3
4	3	2	3
5	3	2	3
6	2		2

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Introduction

Introduction, Architecture, and Microarchitecture, Machine Models, ISA Characteristics, Pipelining Review, Micro-coded Microarchitecture, Pipeline Basics, Structural Hazard, Data Hazards, Memory Technologies, Classification of Caches, Cache Performance

Dependable Memory Hierarchy , Virtual Memory **12 Hours**

Unit II

Memory management and Protection

Memory Management Introduction, Base and Bound Registers, Page Based Memory Systems, Translation, and Protection, TLB Processing, Cache and Memory Protection Interaction

Instructions for Making Decisions , Supporting Procedures in Computer Hardware **12 Hours**

Unit III

Vector Processors and GPUs

Vector Processor Introduction, Vector Parallelism, Vector Hardware Optimizations, Vector Software, and Compiler Optimizations, Reduction, Scatter/Gather, and the Cray, SIMD, GPUs, Multithreading Motivation, Coarse-Grain Multithreading, Simultaneous Multithreading

Hardware Multithreading, Multicore and Other Shared Memory Multiprocessors **12 Hours**

Unit IV

Multiprocessors

Locking Review, Bus Implementation, Cache Coherence, Bus-Based Multiprocessors, Introduction to Interconnection Networks, Message Passing, Interconnect Design, Networking Review, Topology, Topology Parameters, Network Performance, Routing, and Flow Control

SISD, MIMD, SIMD, SPMD, and Vector

12 Hours

Total: 48 Hours

Textbook (s)

1. David A. Patterson, John L. Hennessy, Computer Organization and Design: The Hardware/Software Interface, 3rd edition, The Morgan Kaufmann Series, 2011
2. David A. Patterson, John L. Hennessy, Computer Organization and Design MIPS Edition: The Hardware/Software Interface, 5th edition, The Morgan Kaufmann Series, 2013

Reference (s)

1. Linda Null; Julia Lobur, Essentials of Computer Organization and Architecture Fifth Edition, Jones & Bartlett Learning, 2nd Edition, 2019

Sample Question (S)
Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Examination (%)
Remember	10	10	--
Understand	45	45	--
Apply	45	45	50
Analyze	--	--	50
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. Define pipelining.
2. List few applications of microarchitectures.
3. What is meant by structural hazard?
4. Name any two important memory technologies.

Understand

1. Explain the basic model of page based memory systems.
2. Explain about vector hardware optimization.
3. Explain the key differences between Coarse-Grain Multithreading and Simultaneous Multithreading.

Apply

1. Describe the general characteristics of a program that would exhibit very little temporal and spatial locality with regard to data accesses. Provide an example program
2. If the time for an ALU operation can be shortened by 25%
   a. Will it affect the speedup obtained from pipelining? If yes, by how much? Otherwise, why?
   b. What if the ALU operation now takes 25% more time? **[Open Book Examination]**

Analyze

1. SRAM is commonly used to implement small, fast, on-chip caches while DRAM is used for larger, slower main memory. In the past, a common design for supercomputers was to build machines with no caches and main memories made entirely out of SRAM. If cost were no object, would you still want to design a system this way?
2. A computer architect needs to design the pipeline of a new microprocessor. She has an example workload program core with 106 instructions. Each instruction takes 100 ps to finish.
   a. How long does it take to execute this program core on a nonpipelined processor?
   b. The current state-of-the-art microprocessor has about 20 pipeline stages. Assume it is perfectly pipelined. How much speedup will it achieve compared to the nonpipelined processor?
   c. Real pipelining isn't perfect, since implementing pipelining introduces some overhead per pipeline stage. Will this overhead affect instruction latency, instruction throughput, or both?
   [Open Book Examination]

21FIX01 Full Semester Internship

0 0 0 9

Course Outcomes

1. Use the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems
2. Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences
3. Select appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations
4. Use ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice
5. Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings
6. Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions

COs – POs Mapping

COs	PO_1	PO_2	PO_5	PO_8	PO_9	PO_{10}	PSO_1	PSO_2
1	3	-	-	-	-	-	3	3
2	-	3	-	-	-	-	3	3
3	-	-	3	-	-	-	3	3
4	-	-	-	3	-	-	-	-
5	-	-	-	-	3	-	-	-
6	-	-	-	-	-	3	-	-

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

21ECH11 System on Chip Design

4 0 0 4

Course Outcomes

1. Summarize Silicon on Chip Design
2. Exemplify modelling of bus structure
3. Illustrate the modelling of NoC
4. Compare various power and delay model Approaches
5. Organize different dynamic scaling methodologies
6. Explain Architectural Design exploration

COs – POs Mapping

COs	PO1	PO2	PSO1
1	3		3
2	2		2
3	2	2	2
4	2	3	2
5	3	2	3
6	3		3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit-1: Introduction to Soc design

Case study of SoC – A cell phone, Hardware Design Flow, Levels of system, Modelling Abstraction, Basic SoC Components, Simple Microprocessor: Bus Connection and Internals, A Basic Micro-Controller, UART Device, Programmed I/O, interconnected IP Blocks: simple SoC Bus, RAM – on-chip memory

14 Hours

Unit-2: SoC Architecture:

Bus and Device Structure, Basic Bus: One initiator (II), Basic bus: Multiple Initiators (II), Bridged Bus Structures., Classes of On-Chip Protocol, ARM AXI Bus: The Current Favourite, supporting out-of-order operation using tags, Network on Chip: Simple Ring., Network on-chip: Switch Fabrics., NoC Modelling

15 Hours

Unit-3: Power, Performance and Technology:

Basic Physics, Chip Dissipation, Detailed Delay Model., Detailed Power Model., Dynamic Frequency and Voltage Scaling Example (DVFS), Silicon Power and Technology, 90 Nanometer Gate Length., Power Saving Techniques: Dynamic Clock Gating, Dynamic Supply Gating, Dynamic Frequency Scaling, Dynamic Voltage Scaling, Future Trends

15 Hours

Unit-4: Architectural Design Partition and Exploration:

H/W to S/W Interfacing Techniques, Conservation cores Approach, H/W Design Partition, H/W versus S/W Design Partition Principles, Case study of partitioning: An external RS-232/POTS Modem, Typical Radio/ Wireless Link Structure, Partitioning example: A Bluetooth Module., ASIC costing., Chip cost versus area, Structured ASIC, Xilinx Zynq Super FPGA

16 Hours
Total: 60 Hours

Textbook (s)

1. David J. Greaves, Modern System-on-Chip Design on Arm, 3rd edition, arm education media, 2011
2. Michael J. Flynn, Wayne Luk, Computer System Design: System-on-Chip, Wiley publications, 2011

Reference (s)

1. Kakkar Vipan, System on Chip Design, LAP Lambert Academic Publishing

Sample Question (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Examination (%)
Remember	10	10	--
Understand	45	45	--
Apply	45	45	50
Analyze	--	--	50
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

REMEMBER

1. Define Silicon on Chip Design.
2. List few applications of Silicon on Chip Design.
3. What are the basic SOC components?
4. Name any two power saving techniques.

UNDERSTAND

1. Explain the basic architecture of SoC.
2. Explain characteristics of simple ring and switch fabrics.
3. Explain the key differences between the dynamic clock gating and dynamic supply gating.

APPLY

1. In SOC, what is the difference between One initiator (II) and multiple initiator? Justify each type of basic bus with example.
2. Draw a schematic model of dynamic scaling model and voltage scaling model showing the important components of a typical scaling model. Explain the working of each model using a suitable schematic diagram.
3. Apply the concept of Dynamic Frequency Scaling and Dynamic Voltage Scaling in SoC design and smear out some Future Trends.
4. Apply the design principles to partition the software and hardware in SoC design. Explain using a

suitable circuit diagram how partitioning is performed. **[Open Book Examination]**

ANALYZE

1. Compare various power and delay model Approaches.
2. Organize different dynamic scaling methodologies. **[Open Book Examination]**

21ECH12 CMOS Logic Circuit Design

4 0 0 4

Course Outcomes

1. Interpret the static and dynamic characteristics of CMOS inverter
2. Interpret the electrical behavior of the interconnects and timing issues
3. Compute the power and delay in CMOS circuits
4. Design the combinational CMOS circuits
5. Design the sequential CMOS circuits
6. Outline the designs of memories based on CMOS technology

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PSO_1
1	2	-	-	2
2	2	-	-	2
3	3	2	2	3
4	3	2	2	2
5	3	2	2	3
6	3	2	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Fundamentals of CMOS Inverter circuit

CMOS inverter, static characteristics of CMOS inverter, dynamic characteristics of CMOS inverter, static and dynamic power dissipation, logical effort, inverter delay,, sizing chain of inverters.
Energy & power delay product **14 Hours**

Unit II

Interconnects and Timing issues

Introduction, capacitive parasitics, capacitance and reliability: cross talk, capacitance and performance in CMOS, resistive parasitics, resistance and reliability: ohmic voltage drop, electro migration, resistance and performance: RC delay, synchronous interconnect, asynchronous interconnect, synchronous timing basics.
Sources of skew and jitter, clock-distribution techniques

16 Hours

Unit III

CMOS Subsystem Design

Introduction, adders: combinational adder, transmission gate adder, carry look ahead adder, carry select adder, serial multiplier, parallel multiplier, barrel shifter, SR Latch, clocked latch and flip flop circuits, CMOS D latch , master-slave edge-triggered register.
Synchronous counter , asynchronous counter

16 Hours

Unit IV

Memory Design

Introduction, memory classification, memory architectures and building blocks, the memory core, Read-Only Memories, Nonvolatile Read-Write Memories, Read-Write Memories, Contents-Addressable or Associative Memory, memory peripheral circuitry, address decoders, sense amplifiers, voltage references.
Drivers/buffers, timing and control **14 Hours**

Total: 60 Hours

Text Book (s):

1. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, Digital Integrated Circuits: A Design Perspective, Pearson Education, 2nd Edition,2016.
2. Neil. H. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design: A Systems Perspective, Addison-Wesley Publishing Company, 3rd Edition, 1999.

Reference Book (s):

1. Sung-Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits, Tata McGraw Hill Edition, 3rd Edition,2003.
2. Wayne Wolf, Modern VLSI Design, Prentice Hall, 2nd Edition, 1998.

Sample Question (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	--	--	--
Understand	50	50	--
Apply	50	50	50
Analyse		--	50
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Understand

1. Summarize the effect electromigration in VLSI circuits.

2. Compare between clock skew and jitter.

3. Compare between Latch and Register.

4. Explain the impact of technology node scaling on total power dissipation of SRAM cell.

5. Explain the need of refreshing DRAM Cell at regular intervals.

Apply

1. Demonstrate the working of 6T SRAM cell.

2. Explain Noise margins in CMOS Inverter.

3. Implement a Barrel shifter using CMOS Transistors.

4. Design a 4-bit carry look ahead adder using CMOS logic.

5. Show the essence of Sense Amplifier in Content Addressable Memory.

[Open Examination Question]

Analyse

1. You are designing a clock distribution network in which it is critical to minimize skew between local clocks (CLK1, CLK2, and CLK3). You have extracted the RC net-work of Figure 1, which models the routing parasitics of your clock line. Initially, you notice that the path to CLK3 is shorter than to CLK1 or CLK2. In order to compensate for this imbalance, you insert a transmission gate in the path of CLK3 to eliminate the skew.

a.)Write expressions for the time-constants associated with nodes CLK1, CLK2 and CLK3.Assume the transmission gate can be modeled as a resistance R3.

b.)If R1 = R2 = R4 = R5 = R and C1 = C2 = C3 = C4 = C5 = C, what value of R3 is required to balance the delays to CLK1, CLK2, and CLK3?

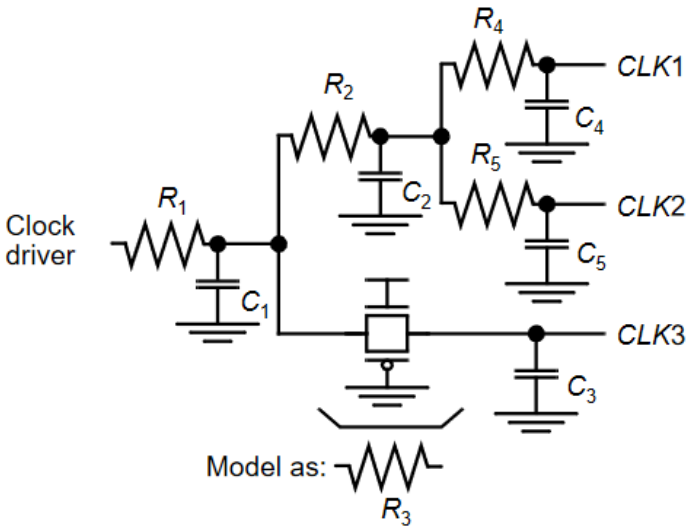


Figure 1 RC clock-distribution network

2. The inverter shown in figure 2 operates with V_{DD}=0.4V and is composed of |Vt| = 0.5V devices. The devices have identical $I_0$and n.

a.) Calculate the switching threshold (VM) of this inverter.

b.)Calculate V_{IL} and V_{IH} of the inverter.

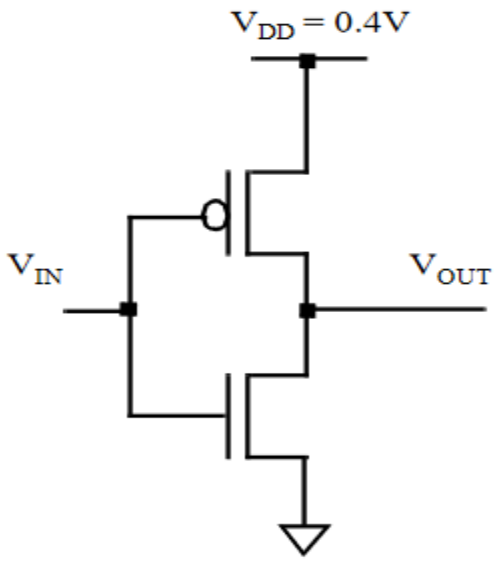


Figure 2: Inverter in Weak Inversion Regime

3. Outline the advantages and disadvantages of arithmetic circuits designed using static CMOS logic and Transmission gates.

4. Justify the requirement of sizing of transistors in VLSI circuits with a suitable example.

5. Justify the tunneling current is higher for NMOS transistors than PMOS transistors with silica gate.
[Open Examination Question]

21ECH13 Low Power VLSI Design

4 0 0 4

Course Outcomes

1. Explain the sources of power dissipation in CMOS
2. Classify the special techniques to mitigate the power consumption in VLSI circuits
3. Demonstrate the power optimization techniques and power dissipation in CMOS circuits
4. Outline the low power circuits
5. Summarize the power optimization and trade-off techniques in digital circuits.
6. Illustrate the power estimation at circuit level

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PSO_1
1	2	-	-	2
2	2	-	-	3
3	3	2	2	3
4	3	2	2	3
5	2	-	-	2
6	2	-	-	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Power Dissipation in CMOS

Sources of power dissipation – Physics of power dissipation in MOSFET devices: The MIS structure, long channel MOSFET, Submicron MOSFET, gate induced drain leakage– Power dissipation in CMOS: short circuit dissipation, dynamic dissipation, load capacitance– Low power VLSI design: Limits – principles of low power design, hierarchy of limits, fundamental limit, material limit.

Device limit, system limit

14 Hours

Unit II

Power Optimization Using Special Techniques

Power Reduction in Clock Networks: Clock Gating, Reduced Swing Clock, Oscillator Circuit for Clock Generation, Frequency Division and Multiplication, Other Clock Power Reduction Techniques - CMOS Floating Node: Tristate Keeper Circuit, Blocking Gate, Low Power Bus: Low Swing Bus, Charge Recycling Bus, Delay Balancing - Low Power Techniques for SRAM: SRAM Cell, Memory Bank Partitioning.

Pulsed Word line and Reduced bit line Swing

16 Hours

Unit III

Design Of Low Power Circuits

Transistor and Gate Sizing : Sizing an Inverter Chain, Transistor and Gate Sizing for Dynamic Power Reduction, Transistor Sizing for Leakage Power Reduction - Network Restructuring and Reorganization: Transistor Network Restructuring, Transistor Network Partitioning and Reorganization - Special Latches and Flip-flops : Self-gating Flip-flop, Combinational Flip-flop, Double Edge Triggered Flip-flop - Low Power Digital Cell Library : Cell Sizes and Spacing.

Varieties of Boolean Functions, Adjustable Device Threshold Voltage

16 Hours

Unit IV

Power Estimation

Modelling of signals - signal probability calculation - Statistical techniques - estimation of glitching power Sensitivity analysis-Power estimation using input vector compaction, power dissipation in Domino logic, circuit reliability, power estimation at the circuit level, Estimation of maximum power: test generation based approach.

steepest descent, generic based algorithm based approach

14 Hours
Total: 60 Hours

Text Book (s):

1. Kiat-Seng Yeo, Kaushik Roy, "Low-Voltage, Low-Power VLSI Subsystems", TMH Professional Engineering.
2. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer,1995
3. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998
4. Rabaey, Pedram, "Low Power Design Methodologies" Kluwer Academic, 1997

5. Neil H. E. Weste, David Money Harris "CMOS VLSI Design 4e: A circuits and systems",Pearson, 2015

Reference Book (s):

1. DimitriosSoudris, Christians Pignet, Costas Goutis, "Designing CMOS Circuits for Low Power", Kluwer, 2002
2. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley 1999
3. AbdelatifBelaouar, Mohamed.I.Elmasry, "Low power digital VLSI design", Kluwer, 1995
4. James B.Kulo, Shih-Chia Lin, "Low voltage SOI CMOS VLSI devices and Circuits", John Wiley and sons, inc. 2001
5. Steven M.Rubin, "Computer Aids for VLSI Design", Addison Wesley Publishing

Sample Question (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember			--
Understand	70	25	--
Apply	30	75	50
Analyse	--		50
Evaluate	--	--	
Create	--	--	--
Total (%)	100	100	100

Understand

1. How parallel processing can be useful in the reduction of power dissipation of a circuit?
2. Explain the switching power dissipation in CMOS circuits.
3. Illustrate various sources of power dissipation in CMOS circuits.
4. Why leakage power dissipation has become an important issue in deep submicron technology?
5. Explain charge recycling in low power VLSI.

Apply

1. Access the importance of low power in the present day VLSI circuit realization?
2. A full wave rectifier is designed with a 50μF capacitor in parallel with a 500Ω resistor. The
3. Demonstrate clocking gating in low power with the help of suitable example.
4. Design a Tristate inverter based Static Master-Slave Flip-Flop.
5. Implement the logic function $F = (PQ + RS + T)'$ using clocked CMOS logic.

[Open Book Examination Question]

Analyse

1. Compare and contrast various leakage techniques used for cache (SRAM).
2. Organize different approaches to design a low-power, low-voltage circuit.
3. Differentiate between short circuit dissipation and dynamic dissipation.
4. Outline the demerits pass transistor and how it can be rectified?
5. Outline the impact of transistor sizing on power consumption and explain with aid of suitable example.

[Open Book Examination Question]

21ECH14 VLSI Fabrication Technology

4 0 0 4

Course Outcomes

1. Explain the methods of crystal growth and epitaxy.
2. Classify the different techniques in Deposition and oxidation
3. Outline the diffusion process in $Si0_2$ and Polycrystalline Silicon
4. Summarize the Ion implantation process and Lithographic techniques.
5. Illustrate Plasma-Assisted and Dry Etching Techniques
6. Demonstrate the methods and problems in Metallization.

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PSO_{13}
1	2	-	-	3
2	2	-	-	3
3	3	2	2	3
4	3	2	2	3
5	2	2	2	3
6	2	-	-	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Crystal Growth, Wafer Preparation and Epitaxy

Electronic-Grade Silicon, Czochralzki Crystal Growing, Silicon Shaping, Vapour-Phase Epitaxy, Molecular Beam Epitaxy

Silicon on Insulators, Epitaxial Evaluation

14 Hours

Unit II

Deposition, Oxidation and Diffusion

Deposition: Deposition Processes, Polysilicon, Silicon Dioxide, Silicon Nitride. Oxidation: Oxidation Techniques and Systems, Oxide Properties, Oxidation of Polysilicon Diffusion: Fick's One-Dimensional Diffusion Equations.

Diffusion in Si02, Diffusion in Polycrystalline Silicon

15 Hours

Unit III

Ion implantation and Lithography

Ion implantation: Ion Implant System and Dose Control, Ion Ranges, Disorder Production, Annealing of Implanted Dopant Impurities. Lithography: Lithographic Process, Optical Lithography.

Electron Beam Lithography, X-Ray Lithography

16 Hours

Unit IV

Etching and Metallization

Etching: Pattern Transfer, Plasma-Assisted Etching Techniques, Control of Etch Rate and Selectivity, Control of Edge Profile, Side Effects, Dry Etching Processes for VLSI Technology. Metallization: Methods of Physical Vapour Deposition, Problems Encountered in Metallization, Metallization Failure.

Corrosion and Bonding

15 Hours

Total: 60 Hours

Text Book (s):

1. Sze, S., VLSI technology. New York: McGraw-Hill Book Company, Second edition, 1988.

Reference Book (s):

1. May, G. S., & Sze, S. M., Fundamentals of semiconductor fabrication. New York: Wiley. 2nd edition 2004.
2. Sorab K. Ghandhi, VLSI Fabrication Principles: Silicon and Gallium Arsenide, Wiley-Interscience-2nd edition, 1994.

Sample Question (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember			--
Understand	70	25	--
Apply	30	75	50
Analyse	--		50
Evaluate	--	--	
Create	--	--	--
Total (%)	100	100	100

Understand

1. How Vapour-Phase Epitaxy is differ from Molecular Beam Epitaxy?
2. Explain Electronic-Grade Silicon process in crystal growth.
3. Why dry oxidation is preferred compared to wet oxidation?
4. Illustrate different types of lithographic techniques
5. Explain dry etching process in VLSI fabrication.

Apply

1. Access the importance of Czochralski Crystal Growing method in fabrication
2. Design Fick's One-Dimensional Diffusion Equations.
3. A 10-μA ion beam has a 10° half-angle divergence as it passes through a square aperture (8 cm x 8 cm), placed 6 cm away from the target. Using a current meter, how much time is needed to implant $l0^3$ atoms/cm^2 for (a) a singly ionized, monatomic species, (b) a triply ionized diatomic species? Using a charge integrator (measures It) calibrated for a singly ionized monatomic species, (c) what dose should be "set" to obtain $l0^{13}$ atom/cm" for the triply ionized diatomic species?
4. In electron beam lithography the term Gaussian beam diameter (d_G) describes the diameter of an electron beam in the absence of system aberrations, that is, a beam distorted only by the thermal velocities of the electrons. The current density in a Gaussian beam is given hy $J = J_p \exp [— (r/\sigma)^2]$, where J_p is the peak current density, r is the radius from the center of the beam, and σ is the standard deviation of electron distribution in the beam. Defining $d_G = 2\sigma$, derive an expression relating d_G to the peak current density J_p and the total current in the electron beam I.
5. Built a Plasma-Assisted Etching Techniques to control of Etch Rate and Selectivity.

[Open Book Examination Question]

Analyse

1. Organize different approaches to Epitaxial Evaluation.
2. Differentiate between Diffusion in Si02 and Diffusion in Polycrystalline Silicon.
3. Compare and contrast various lithographic techniques used in VLSI fabrication.
4. The maximum current density J_m, that can be focused toward a spot with a convergence half-angle a is limited by the transverse thermal emission velocities of the electrons in a Gaussian electron beam. For small convergence angles, derive an expression that relates the Gaussian beam diameter dG to the electron source parameters J_c ,T_c , and V_0.
5. Examine the problems Encountered in Metallization

[Open Book Examination Question]

21ECH21 Advanced Controllers

4 0 0 4

Course Outcomes

1. Illustrate the architecture of PIC microcontroller
2. Outline the instruction set of PIC microcontroller
3. Carry-out the programming of PIC microcontroller
4. Illustrate the architecture of ARM processor
5. Outline the instruction set of ARM processor
6. Carry-out the programming of ARM processor

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PSO_1
1	2	-	-	-
2	3	2	2	3
3	3	2	2	3
4	2	-	-	-
5	3	2	2	3
6	3	2	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

PIC Microcontrollers

RISC vs CISC, Harvard and Von Neumann architecture, introduction to PIC microcontrollers, PIC18F family microcontroller architecture, support devices, microchip PIC family of devices, PIC18 interrupts, PIC18 timers and interfacing,

input/output ports **14 Hours**

Unit II

PIC Microcontrollers Programming

PIC18F programming model, Instruction set: data copy, arithmetic, branching, bit manipulation.

Stack and subroutine, Integrated Development Environment (IDE), application programs and software design

Study of *Hex file, list file*

15 Hours

Unit III

ARM Processors Architecture

Introduction to ARM processors cores, registers, Current Program Status Register, pipeline, exception, interrupt, interrupt vector table, core extensions, architecture revision, ARM processor families, ARM 7TDMI and ARM9TDMI processors, interfacing ARM 7TDMI and ARM9TDMI processors to other devices.

Applications of ARM 7TDMI and ARM9TDMI processors

15 Hours

Unit IV

ARM Processor Programming

ARM Instructions set, thumb instructions set, writing and optimizing ARM assembly code, design issues, assembly programming in ARM, architectural support for system development, optimized primitives, exception and interrupt handling, caches memory protecting units, memory management units, embedded operating system using in the ARM

Antilock breaking system, Elevator control system **16 Hours**

Total: 60 Hours

Text Book (s):

1. Ramesh Gaonkar, Fundamentals of Microcontrollers and Applications in Embedded Systems, Penram International Publishing (India)Pvt. Ltd.,2007, 1st ed.
2. Andrew N Sloss, Dominic Symes and Chris Wright, ARM systems developer's guide, Elsevier, 2004.

Reference Book (s):

1. lucio Bi Jasio, PIC microcontrollers, Newnes Publishers.
2. Trevor Martin, The insider's guide of the Philips ARM7 based microcontrollers, Hitex (UK), 2005

Sample Question (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	10	10	--
Understand	25	25	--
Apply	50	50	50
Analyse	15	15	50
Evaluate	--	--	
Create	--	--	--
Total (%)	100	100	100

Remember

1. List the two primary modes of data transfer.
2. List sources that can interrupt the PIC18F.
3. State the advantage of EEPROM over flash memory.
4. Recall the number of bits required for a Thumb instruction of an ARM microcontroller?

Understand

1. Explain the interrupt process.
2. Explain the features of RISC Machine.
Explain about the register file of ARM processor.
3. Explain about the register file of ARM processor.
4. Explain various modes of ARM processor.

Apply

1. Write a program for PIC18F to copy the following seven data bytes from program memory to data registers starting from REG26 (0×26) in the reverse order.
Data Bytes (H): 72, F2, 82, 68, 49, 7F, 9C
2. Write a program for PIC18F to setup the CCPI in PWM mode to generate a pulse waveform at 10 kHz with a 40% duty cycle if the crystal frequency is 10 MHz.
3. Write a program for PIC18F to generate a trigger as a special event every 10 ms that can be used initiate an A/D conversion if the crystal frequency is 10 MHz.

[Open book question]

Analyse

1. Compare and contrast RISC and CISC architectures.
2. A branch instruction changes the flow of execution or is used to call a routine. Differentiate between the ARMv5E branch instructions as given below:
Syntax: B{<cond>} label
BL{<cond>} label
BX{<cond>} Rm
BLX{<cond>} label | Rm
3. Interface four PIC18F452 microcontroller using PORTB and PORTC, and outline how the circuit works. Write instructions to display a four-digit number (or a four-character message) stored in data registers starting from REG20 (address 20H).

[Open book question]

21ECH22 Robots and Control

4 0 0 4

Course Outcomes

1. Explain fundamentals of the robotics
2. Compute the robot motion through forward kinematics
3. Compute the robot motion through inverse kinematics
4. Access the robotic sensors
5. Access the robotic vision
6. Summarize the robotic applications

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PSO_1
1	2	-	-	2
2	3	2	2	3
3	3	2	2	3
4	3	2	2	3
5	3	2	2	3
6	2	-	-	2

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Introduction to Robotics

Evolution of robot and robotics, law of robotics, progressive advancements in robots, robot anatomy, human arm characteristics, design and control issues, manipulation and control, Actuators: Electric actuators, hydraulic actuators, pneumatic actuators, selection of motors, Grippers. Coordinate frames.
mapping and transforms of grippers **13 Hours**

Unit II

Robot Modeling

Mechanical structure and notations, links and joints, kinematic modelling of manipulator, Denavit-Hartenberg notation, kinematic relationship between adjacent links, manipulator transformation matrix.
Inverse kinematic: manipulator workspace, solvability of inverse kinematic model.
Dynamic modelling: Lagrangian mechanics, Lagrange-Euler formulation, Newton-Euler formulation.
solution techniques, closed form solution

16 Hours

Unit III

Robotic sensor, vision and signal conditioning

Sensing, sensors in Robotics: status sensors, environment sensors, quality control sensors, safety sensors, workcell control sensors, acoustic sensors, optics sensors, pneumatic sensors, force/torque, optical encoders. Robotic vision, industrial applications of vision controlled robotic systems: presence, object location, pick and place, object identification, visual inspection, visual guidance. Architecture of robotic vision systems.
image acquisition, signal conditioning

16 Hours

Unit IV

Industrial Robots and it's Applications

Robot Subsystem: motion sub system, recognition subsystem, control sub system. Classification of robots based on coordinate systems, Industrial applications: material handling applications, processing applications, assembling applications, inspection applications. Non-industrial applications.
justification of robots, robot safety **15 Hours**

Total: 60 Hours

Text Book (s):

1. R K Mittal and Nagrath, Robotics and Control, Tata McGraw-Hill Education, 1st Edition, 2003
2. S K saha, Introduction of Robotics, McGraw-Hill Education (India) Private Ltd., 2nd Edition, 2008.

Reference Book (s):

1. Philippe Coiffet, Michael Chirouze, An Introduction to Robot Technology, Springer Science & Business Media, Illustrated Edition, 2012 .
2. K S Fu, Ralph Gonzalez, C S G Lee, Robotics: Control Sensing. Vision, and Intelligence, Tata McGraw1Hill Education, 2nd Edition, 2008

3. M P Groover, Industrial Robotics (Special Indian Edition), Tata McGraw-Hill Education, 2nd Edition, 2012.

Sample Question (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	--	--	--
Understand	25	15	--
Apply	50	35	50
Analyse	25	50	50
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. Define the terms 'Robot' and 'Robotic'.
2. What are the main characteristics of a robot?
3. Define the law of robotics.
4. List four basic components of robot.
5. List four typical applications of robot.

Understand

1. Explain the various robot configurations with neat sketches.
2. Briefly explain the four basic configurations of arm in robotic manipulator.
3. Illustrate the use of ADC and DAC in a robot.

Apply

1. Discuss the role of robots in engineering.
2. Obtain the direct kinematics equation of the 4-DOF Selective Compliance Assembly Robot Arm (SCARA) robots.

[Open book question]

Analyse

1. Outline a state of art report on robotics in India.
2. What are future manufacturing applications of robot?
3. A robot is required to perform the assembly of a shaft into a bearing placed in an arbitrary position. How many degrees of freedom is required for a manipulator to perform this task? If the bearing is placed in a fixed, say a horizontal plane, what will be the required number of degrees of freedom. Justify your answer.

[Open book question]

21ECH23 Industrial Automation

4 0 0 4

Course Outcomes

1. Illustrate the importance of automation techniques manufacturing and process industries..
2. Predict the role of PLC in industry automation.
3. Interpolate various control techniques employed in process automation.
4. Predict the role of Distributed Control System in industry automation.
5. Asses the importance of Automated Inspection Principles and sensor technology
6. Implement various applications of robots

COs – POs Mapping

COs	PO_1	PO_2	PSO_1	PSO_2
1	2	2	3	3
2	2	2	3	3
3	3	3	3	3
4	2	3	3	3
5	3	3	3	3
6	3	3	3	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit – I

Introduction to computer based industrial automation- Direct Digital Control (DDC), Distributed Control System (DCS) and supervisory control and data acquisition (SCADA) based architectures. SCADA for process industries includes understanding of RTUs, Pumping stations, Evacuation processes, Mass Flow Meters and other flow meters.

Leak-flow studies of pipelines, Transport Automation **14 Hours**

Unit-II

Programmable Logic Controller (PLC)- Block diagram of PLC, Programming languages of PLC, Basic instruction sets, Design of alarm and interlocks, Networking of PLC, Overview of safety of PLC with case studies. Process Safety Automation: Levels of process safety through use of PLCs, Integrating Process safety PLC and DCS

Application of international standards in process safety control **15 Hours**

Unit – III

Distributed Control System- Local Control Unit (LCU) architecture, LCU Process Interfacing Issues, Block diagram and Overview of different LCU security design approaches, Networking of DCS. Introduction to communication protocols- Profibus, Field bus, HART protocols, Real-time analysis of data stream from DCS, Historian build, Integration of business inputs with process data, Leveraging RTU (as different from PLCs and DCS)

Data gathering, Data analytics **15 Hours**

Unit – IV

Automated Inspection and Testing: Automated Inspection Principles and Methods, Sensor Technologies for Automated Inspection, Coordinate Measuring Machines, Other Contact Inspection Methods, Machine Vision, Other optical Inspection Methods. Robotic vision systems, image representation, object recognition and categorization, depth measurement, image data compression, visual inspection Application of Robots in welding, Spray painting, assembly operation.

cleaning, robot for underwater applications

16 Hours

Total Hours 60

Text Book (s):

1. M.P.Groover,"Automation, Production Systems and Computer Integrated Manufacturing", 5 th Edition, Pearson Education, 2009.
2. John W. Webb and Ronald A. Reis, "Programmable Logic Controllers: Principles and Applications", 5th Edition, Prentice Hall Inc., New Jersey, 2003.
3. Deb S R and Deb S, —Robotics Technology and Flexible Automation, Tata McGraw Hill Education Pvt. Ltd, 2010.

4. Mikell P Groover, "Automation, Production Systems, and Computer-Integrated Manufacturing", Pearson Education, 2015.

Reference Book (s):

1. Frank D. Petruzella, "Programmable Logic Controllers", 5th Edition, McGraw- Hill, New York, 2016.
2. Guanrong Chen, Trung Tat Pham, Chapman & Hall/CRC, Introduction to Fuzzy Systems, 2009.
Ashitava Ghoshal, Robotics-Fundamental Concepts and Analysis', Oxford University Press, Sixth impression, 2010.

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	10	--	--
Understand	25	15	--
Apply	50	35	50
Analyse	15	50	50
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. Mention the requirements of automation.
2. List different input and output devices used in control systems
3. State the advantages of PLC.

Understand

1. Explain about Distributed Control System (DCS) and supervisory control
2. Represent the architecture of Local Control Unit (LCU)
3. Identify the Application of international standards in process safety control

Apply

1. Construct the Block diagram and Overview of different LCU security design approaches
2. Demonstrate the HART protocols
3. Demonstrate the robot for underwater applications

[Open book question]

Analyze

1. Compare Direct Digital Control (DDC), Distributed Control System (DCS)
2. Outline the process of sensor technology for automation inspection
3. Tine the process of depth measuring

[Open book question]

21ECH24 Distributed Embedded Systems

4 0 0 4

Course Outcomes

1. Understand the design principles of distributed embedded systems
2. Classify the of real time embedded systems
3. Demonstrate the Modeling of Real Time Systems.
4. Illustrate the Real Time Entities and Images Real time Entities in embedded systems
5. Outline the design CAN network based systems
6. Summarize the CAN and CAN open networking features.

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PSO_1
1	2	-	-	2
2	2	-	-	3
3	3	2	2	3
4	3	2	2	3
5	2	-	-	2
6	2	-	-	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

REAL-TIME ENVIRONMENT

The Real Time Environment Overview Introduction, Functional Requirements, Temporal Requirements, Dependability Requirements, Classification of Real Time systems The Real Time systems Market, Examples of Real Time systems. Distributed System Overview System Architecture, Compensability, Scalability, Dependability Physical Installation. Real-time computer system requirements – classification of real time systems – simplicity – global time – real time model.

internal and external clock synchronization **14 Hours**

Unit II

Real time Operating systems

Real – time communication – temporal relations – dependability – power and energy awareness – real –time communication – event triggered – rate constrained – time triggered. Inter component communication – task management – dual role of time – inter task interactions – process input/output – agreement protocols – error detection. Global Time Overview Time and Order, Time Measurements, Dense Time versus sparse Time.

Internal Clock synchronization, External clock synchronization

16 Hours

Unit III

Modeling Real Time Systems

Appropriate Abstractions, The Structural Elements, Interfaces, Temporal Control, Worst case Execution Time. Real Time Entities and Images Real time Entities, Real Time Image and Objects, Temporal accuracy. F *Permanence and Idem potency ault Tolerance.*

14 Hours

Unit IV

Time Triggered Protocol and Control Area Network (CAN)

Introduction to CAN Open – CAN open standard – Object directory – Electronic Data Sheets & Devices. Configuration Files – Service Data Objectives – Network management CAN open messages – Device Profile Encoder. Introduction to TTP, Overview, Protocol Layers, Internal Operations of TTP/C, TTP/A for Field Bus. *Applications, Advanced topic on distributed embedded system*

16Hours

Total: 60 Hours

Text Book (s):

1. Kopetz, Hermann. Real-time systems: design principles for distributed embedded applications. Springer Science & Business Media, 2011.
2. Hermann Kopetz, "Real–Time systems – Design Principles for distributed Embedded Applications", 2nd Edition, Springer 2011.
3. Glaf P.Feiffer, Andrew Ayre and Christian Keyold, "Embedded Networking with CAN and CAN open", Copperhill Media Corporation, 2008.

Reference Book (s):

1. Herma K., "Real Time Systems – Design for distributed Embedded Applications", Kluwer Academic,

1997.
2. C.M. Krishna, Kang, G.Shin, "Real Time Systems", McGraw Hill, 1997
3. Andrew S. Tanenbaum, "Distributed operating systems", Pearson 2013
4. Ajay D Kshemkalyani,Mukesh Singhal, "Distributed Computing" – Principles, Algorithm and systems, Cambridge university press 2008

Sample Question (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember			--
Understand	70	25	--
Apply	30	75	50
Analyse	--		50
Evaluate	--	--	
Create	--	--	--
Total (%)	100	100	100

Understand

1. Summarize the functional requirements of Real Time Systems.
2. Classify the real time systems.
3. Illustrate system architecture of distributed systems.
4. Indicate the CAN Open features.
5. Explain Internal Clock synchronization in distributed systems.

Apply

1. Access the importance of Time Triggered Protocol in Field Bus Applications?
2. Predict Temporal accuracy of real time systems.
3. Demonstrate Worst case Execution Time in real time systems with the help of suitable example.
4. Design a distributed embedded system using CAN.
5. Demonstrate the Structural Elements of Distributed real time systems.

[Open Book Examination Question]

Analyse

1. Compare and contrast various Dense Time and sparse Time in RTOS.
2. Organize different approaches to task management in RTOS.
3. Differentiate between Internal Clock synchronization and External clock synchronization.
4. Outline the demerits TTP and how it can be rectified?
5. Outline the Worst case Execution Time and explain with aid of suitable example.

[Open Book Examination Question]

21ECH31 Optical Communications

4 0 0 4

Course Outcomes

1. Recall basic optical laws, definitions and explain optical fiber structures, waveguides.
2. Illustrate signal degradation in optical fibers
3. Demonstrate LED and laser optical sources.
4. Demonstrate photo detectors and optical receiver operation.
5. Interpret optical link design methods.
6. Illustrate the methods for Measurement of attenuation and dispersion

COs – POs Mapping

COs	PO_1	PO_2	PSO_2
1	2	-	2
2	2	-	2
3	3	2	3
4	3	2	3
5	2	-	2
6	2	-	2

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Introduction to Optical Fiber Communication

Overview of optical fiber communication - Historical development, the general system, advantages of optical fiber communications. Optical fiber wave guides- Introduction, Ray theory transmission, Total Internal Reflection, Acceptance angle, Numerical Aperture, Skew rays. Cylindrical fibers- Modes, V-number, Mode coupling, Step Index fibers, Graded Index fibers.Single mode fibers- Cut off wavelength, Mode Field Diameter, Effective Refractive Index. Fiber materials — Glass, Halide, Active glass, Chalgenide glass, Plastic optical fibers. Signal distortion in optical fibers- Attenuation, Absorption, Scattering and Bending losses.

Core and Cladding

16 Hours

Unit II

Optical Sources

Fiber dispersion Information capacity determination, Group delay, Types of Dispersion – Material dispersion, Wave-guide dispersion, Polarization mode dispersion, Intermodal dispersion. Pulse broadening. Optical fiber Connectors- Connector types. Fiber Splicing- Splicing techniques, splicing single mode fibers. Fiber alignment and joint loss- Multimode fiber joints, single mode fiber joints. Optical sources- LEDs, Structures, Materials, Quantum efficiency, Power, Modulation, Power bandwidth product. Injection Laser Diodes- Modes, Threshold conditions, resonant frequencies.

External quantum efficiency, and Laser diode rate equations

15 Hours

Unit III

Photodetectors

Source to fiber power launching - Power coupling, Power launching, Equilibrium Numerical Aperture, Optical detectors- Physical principles of PIN and APD, Detector response time, Temperature effect on Avalanche gain, Comparison of Photodetectors. Optical receiver operation- Fundamental receiver operation, Digital signal transmission, error sources, Receiver configuration, Digital receiver performance, Probability of error.

Quantum limit, Analog receiver **15 Hours**

Unit IV

Optical System Design

Optical system design —Considerations, Component choice, Multiplexing. Point-to- point links, Systemconsiderations, Link power budget with examples. Overall fiber dispersion in Multi mode and Single mode fibers, Rise time budget with examples. Line coding in Optical links, WDM, Necessity, Principles, Types of WDM, Eye pattern.

Measurement of Attenuation and Dispersion **14 Hours**

Total: 60 Hours

Text Book (s):

1. John M. Senior, Optical Fiber Communications, 2nd Edition, PHI, 2002
2. Gerd Keiser, Optical Fiber Communications, 3rd Edition, Mc Graw-Hill International edition, 2000

Reference Book (s):

1. D.K. Mynbaev ,S.C.Gupta and Lowell L. Scheiner, Fiber Optics Communications, Pearson Education, 2007.
2. S.C.Gupta, Text Book on Optical Fibre Communication and its Applications, PHI, 2007.
3. Govind P. Agarwal, Fiber Optic Communication Systems, John Wiley, 3rd Edition, 2004.
4. Joseph C. Palais, Fiber Optic Communications, Pearson Education, 4th Edition, 2004.

Sample Question (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	25	25	--
Understand	50	50	--
Apply	25	25	25
Analyse	--	--	75
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Remember

1. Define Numerical Aperture
2. List any four materials used for fiber manufacturing.
3. Explain WDM

Understand

1. Explain the advantages of Optical fiber communication.
2. Explain material dispersion and waveguide dispersion
3. Illustrate fiber splicing techniques
4. Explain fundamental Receiver operation in optical system

Apply

1. Design optical system using link power budget. Explain with an example
2. The quantum efficiency of an In GaAs PIN diode is 80% in the wave length range between 1300nm and 1600nm. Compute the range of responsivity of the PIN diode in the specified wavelength range.
3. Explain types of error sources in detection mechanism.
4. A multimode graded index fiber exhibits total pulse broadening of 0.1μs over a distance of 15Km. Find its maximum possible bandwidth and pulse dispersion per unit length.

[Open Book Examination Question]

21ECH32 MIMO Wireless Communications

4 0 0 4

Course Outcomes

1. Illustrate Multiple Input Multiple Output (MIMO) Communication Systems
2. Illustrate the fading channel models and Power allocation algorithms in MIMO
3. Find capacity of different MIMO Channels.
4. Demonstrate various space time coding techniques.
5. Outline different signal detection methods in MIMO Communication
6. Compare MIMO Systems with Single Input Single Output (SISO) Systems.

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PSO_2
1	2	1	1	3
2	2	1	1	3
3	3	2	2	3
4	3	2	2	3
5	3	3	3	3
6	3	3	3	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Introduction to MIMO Systems

Diversity in wireless communications, Wireless fading channel characteristics, Advantages and Applications of MIMO systems, Fading Channel Models: Uncorrelated - fully correlated - separately correlated - keyhole MIMO fading models, parallel decomposition of MIMO channel.

Power allocation in MIMO: Uniform - adaptive -near optimal power allocation **14 Hours**

Unit II

MIMO Channel Capacity

Capacity for deterministic MIMO Channels: SISO – SIMO – MISO – MIMO, Capacity of random MIMO channels: SISO – SIMO – MISO – MIMO (Unity Channel Matrix, Identity Channel Matrix), Capacity of independent identically distributed channels, Capacity of separately correlated Rayleigh fading MIMO channels.

Capacity of keyhole Rayleigh fading MIMO channel

16 Hours

Unit III

Introduction to Space-Time Codes

Advantages, code design criteria, Alamouti space-time codes, SER analysis of Alamouti space-time code over fading channels, Space-time block codes, Space-time trellis codes, Performance analysis of Space-time codes over separately correlated MIMO channel, Space-time turbo codes, BLAST Architectures: VBLAST – HBLAST. *SCBLAST - DBLAST*

16 Hours

Unit IV

MIMO Detection Techniques

Maximum Likelihood, Zero Forcing, Minimum Mean Square Error, Zero Forcing Equalization with Successive Interference Cancellation, Minimum Mean Square Error Successive Interference Cancellation, Lattice Reduction based detection, Introduction to spatially multiplexed MIMO systems, Vertical/horizontal layered space-time transmission.

Diagonal Bell labs layered space-time transmission

14 Hours

Total: 60 Hours

Text Book (s):

1. R. S. Kshetrimayum, "Fundamentals of MIMO Wireless Communications", Cambridge University Press, 2017.
2. Tolga M. Duman and Ali Ghrayeb, "Coding for MIMO Communication Systems", John Wiley & Sons Ltd., 2007.
3. Tse, D. and Viswanath, P., Fundamentals of wireless communication, Cambridge University Press, 2005
4. Goldsmith, A., Wireless Communications, Cambridge University Press, 2005
5. Mohinder Janakiram, "Space time Processing and MIMO systems", Artech House, First Edition, 2004

Reference Book (s):

1. Ezio Biglieri, Robert Calderbank et al "MIMO Wireless Communications" Cambridge University

Press 2007
2. B. Kumbhani and R. S. Kshetrimayum, "MIMO Wireless Communications over Generalized Fading Channels", CRC Press, 2017.
3. T. L. Marze_a, E. G. Larsson, H. Yang and H. Q. Ngo, "Fundamentals of Massive MIMO", Cambridge University Press, 2016.
4. Hamid Jafarkhani, "Space Time coding-Theory and Practice", Cambridge University Press, First Edition, 2005.
5. Branka Vucetic and Jinhong Yuan, "Space Time coding", John Wiley and Sons, First Edition, 2003.

Sample Question (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	--	--	--
Understand	70	25	--
Apply	30	75	50
Analyse	--	--	50
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Understand

1. Illustrate the two gains we can achieve from MIMO systems taking example for 4×4 MIMO system. Assume rich Rayleigh scattering environment.
2. Illustrate frequency-flat, frequency-selective, fast and slow fading channels.
3. Represent the ergodic and outage capacity for i.i.d. uncorrelated classical fading SIMO channel whose fading distribution is (a) Nakagami-m (b) Hoyt (c) Weibull.
4. Illustrate Maximum Likelihood detection technique.
5. Represent Alamouti space-time code.

Apply

1. Show that the diversity order of MMSE detector for a i.i.d. Rayleigh fading channel is $N_R - N_T + 1$?
2. Find the ergodic and outage capacity for i.i.d. uncorrelated generalized fading SIMO channel whose fading distribution is α-μ distributed.
3. Show that $\mathrm{vec}(AB) = (B^T \otimes I)\,\mathrm{vec}(A)$.
4. Find the spectral efficiency and best power allocation for the MIMO channel whose
$$H = \begin{bmatrix} 0.1 & 0 & 0 \\ 0 & 0.5 & 0 \\ 0 & 0 & 0.9 \end{bmatrix}$$ assuming $\gamma = \frac{\rho}{\sigma^2} = 10\text{dB}$ and BW= 1Hz .
5. Demonstrate the key performance-deciding parameters of MIMO channel capacity for high and low SNR cases.

[Open Book Examination Question]

1. Consider the n-dimensional standard Gaussian random vector $w \sim N(0, I_n)$ and its squared magnitude $\|w\|^2$, (a) with n = 1, show that the density of $\|w\|^2$ is
$$f_1(a) = \frac{1}{\sqrt{2\pi a}} \exp\left(-\frac{a}{2}\right), \quad a \geq 0$$
(b) For any n, show that the density of $\|w\|^2$ (denoted by $f_n(\cdot)$) satisfies the recursive relation:
$$f_{n+2}(a) = \frac{a}{n} f_n(a), \quad a \geq 0$$

Analyse

1. Compare Space time block codes and Space time trellis codes.
2. Is ML detection gives better performance than ZF detection, Justify?
3. Differentiate between short circuit dissipation and dynamic dissipation.
4. Outline the VBLAST architecture.
5. Contrast SISO, SIMO, MISO, MIMO.
6. Consider a complex Gaussian random vector x. necessary and sufficient condition for x to be circular symmetric is that the mean μ and the pseudo-covariance matrix J are zero. Justify?

[Open Book Examination Question]

21ECH33 Software Defined Radio

4 0 0 4

Course Outcomes

1. Illustrate the Architecture of Software Defined Radio
2. Demonstrate digital filters and multi rate processing
3. Outline various digital frequency convertors.
4. Differentiate the transmitter and receiver architectures
5. Implement SDR for a various application
6. Attribute the parameters of smart antenna

COs – POs Mapping

COs	PO1	PO 2	PSO_2
1	2	-	2
2	3	3	3
3	3	3	3
4	3	3	3
5	3	3	3
6	3	3	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit-I

SDR Architecture

Software Defined Radio: A Traditional Hardware Radio Architecture, Signal Processing Hardware: Introduction to 2G Radio Architectures, Hybrid Radio Architecture, Basic Software Defined Radio Block Diagram, System Level Functioning Partitioning, , RF System Design: Noise and Channel Capacity, Receiver Requirements.

Signal Processing Capacity Tradeoff

15 Hours

Unit-II

Digital Frequency Converters

Digital Conversion Fundamentals, Sample Rate, Band pass sampling, oversampling, Anti-alias Filtering, Frequency converter Fundamentals, Digital NCO, Digital Mixers, and Digital Filters: Half band Filters, CIC Filters Decimation, Interpolation, and Multirate Processing, DUCs Cascading, Digital Converters and Digital Frequency Converters.

Figure of Merit-DACs- DAC Noise Budget- ADC Noise Budget

15 Hours

Unit-III

Signal Processing Hardware Components:

Introduction to SDR Requirements for Processing Power, DSP Devices, DSP Compilers, Reconfigurable Processors, Adaptive Computing Machine, FPGAs Software Architecture and Components, Architecture Choices: Hardware, Specific Software Architecture.

Software Standards for SDR

15 Hours

Unit-IV

Smart Antennas Using Software Radio

3G smart Antenna Requirements, Phased Antenna Array, Software Radio Principles to Antenna Systems, Smart Antenna Architectures, Optimum combining, Adaptive Arrays, DOA Arrays, Beam Forming for CDMA.

Downlink Beam Forming

15 Hours

Total: 60 Hours

Textbook (s)

1. Paul Burns, Software Defined Radio for 3G, Artech House, 2002
2. Tony J Rouphael, RF and DSP for SDR, Elsevier Newnes Press, 2008
3. JoukoVanakka, Digital Synthesizers and Transmitter for Software Radio, Springer, 2005

Reference (s)

1. Eugene Grayver, Implementing Software Defined Radio, Springer-Verlag New York, 2013.
2. Walter Tuttlebee, Software Defined Radio Enabling Technologies, John Wiley & Sons, Ltd,2002
3. P Kenington, RF and Baseband Techniques for Software Defined Radio, Artech House, 2005

SAMPLE QUESTION (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	35	15	--
Understand	30	20	--
Apply	35	35	50
Analyse	-	-	50
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

REMEMBER

1. State hybrid architecture
2. List different types of architecture
3. Define Channel Capacity
4. List the primary reasons that the military sector might embrace the open architecture SDR

UNDERSTAND

1. Explain the Spectrum management Implications in SDR
2. Illustrate the ideal Software Radio with an example
3. Illustrate the principals of smart antenna
4. Compare different types of antennas used in 3G communications

APPLY

1. Implement half band filter and mention the application of it
2. Determine SDR Requirements for Processing Power
3. Construct an adaptive computing machine

[Open book question]

ANALYZE

1. Analyze the SDR software architecture
2. Justify how logical layers related to physical code
3. Compare software architecture from radio architecture.

[Open book question]

21ECH34 Wireless Mobile Networks

4 0 0 4

Course Outcomes

1. Explain the wireless transmission fundamentals
2. Summarize the basic principles of various radio access networks
3. Outline the network architecture of GSM system
4. Summarize the mobile network layer issues
5. Illustrate the mobile IP configuration protocols
6. Demonstrate the performance of mobile transport layer using congestion control protocols

COs – POs Mapping

COs	PO_1	PO_2	PSO_1
1	-	-	3
2	2	-	3
3	2	2	3
4	2	2	3
5	2	2	3
6	2	-	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Wireless transmission

Introduction to Wireless mobile networks and its applications; Frequencies for radio transmission-Signals-Antennas-Signal propagation-multiplexing-Modulation-
Spread spectrum-Cellular systems

14 Hours

Unit II

Telecommunications systems

Motivation for a specialized MAC-SDMA-FDMA-TDMA-CDMA-Comparison of S/T/F/CDMA IS-95, CDMA2000 1X/3X-WCDMA (3G). GSM-Mobile services-system architecture, radio interface, protocols, localization and calling, New data services- GPRS,EDGE (2.5G),UMTS and IMT-2000 (3G). (4G) LTE radio access-basic principles.
Handover, Security

16 Hours

Unit III

Mobile Network layer

Mobile IP-Goals and requirements, entities and terminology, IP packet delivery, Agent discovery, Registration, Tunneling and encapsulation, optimizations, IPV6 343, IP micro-mobility support; Dynamic host configuration protocol.
Mobile ad-hoc networks.

14 Hours

Unit IV

Mobile Transport layer

Traditional TCP- Congestion control, Slow start, Fast retransmit/fast recovery, Implications of mobility; Classical TCP improvements-Indirect TCP 375, Snooping TCP 378, Mobile TCP 380, Fast retransmit/fast recovery 382, Transmission/time-out freezing 383, selective retransmission 383, Transaction-oriented TCP 384, TCP over 2.5/3G wireless networks
Performance enhancing proxies.

16 Hours
Total: 60 Hours

Text Book (s):

1. Mobile Communication, Jochen Schiller, Second Edition, PEARSON Education,2003

Reference Book (s):

1. Theodore S.Rappaport, "Wireless Communications principles and practice", second edition, Prentice Hall of India, 2006
2. K. Pahlavan and A. Levesque, "Wireless Information Networks", John Wiley and Sons, second edition, 2005

Sample Question (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam[1] (%)
Remember	--	--	--
Understand	70	25	--
Apply	30	75	50
Analyse	--	--	50
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Understand

1. Differentiate FDMA and TDMA.
2. Explain how tunnelling works in general for mobile IP?
3. Explain the new elements added to the GSM infrastructure to support GPRS.

Apply

1. GSM has 125 forward channels and 125 reverse channels with each channel having a bandwidth of 200 kHz. Find the bandwidth in the uplink and downlink frequency band, if each channel is subdivided into 16 time lots determine the sub channel spacing.
2. The bit stream of an OQPSK is 001010100110. Assume that the bit rate f_b is half the carrier frequency f_c. Sketch the output of OQPK and show if odd bit stream is delayed by T_b, QPSK is generated.

[Open Book Examination Question]

Analyse

1. Suppose that you work with a cellular service provider and the cellular radio system deployed by the company in a given service area just reached its maximum system capacity. Outline the various techniques to increase the capacity of the existing network,
2. What limits the number of simultaneous users in a TDM/FDM system compared to a CDM system? What happens to the transmission quality of connections if the load gets higher in a cell, i.e. how does an additional user influence the other users in the cell?

[Open Book Examination Question]

21ECH41 Optimization Techniques

4 0 0 4

Course Outcomes

1. Exemplify the concept of soft computing techniques and their roles in building intelligent machines.
2. Differentiate supervised and unsupervised learning methods to different neural networks models for pattern classification and regression problems.
3. Demonstrate the concept of fuzzy set and relatonships.
4. Carry-out fuzzy logic and reasoning to handle uncertainty and solve engineering problems.
5. Implement the Support Vector Machines to classify objects in real time applications.
6. Compare solutions by various soft computing approaches for a given problem.

COs – POs Mapping

COs	PO_1	PO_2	PSO_1	PSO_2
1	2	-	2	2
2	3	3	3	3
3	3	2	3	3
4	3	2	3	3
5	3	2	3	3
6	3	3	3	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Introduction to Soft Computing and Artificial Neural Networks Introduction to soft computing, Fuzzy logic, Neural Networks and Evolutionary Computing, Approximations of Multivariate functions, Non – linear Error surface and optimization. Introduction to ANN, Basic models of ANN, important terminologies, Basic Learning Laws, Supervised Learning Networks, Perceptron Networks, Adaptive Linear Neuron, Back propagation Network Radial basis function network and Hopfield Networks.
Bi-directional associative memories

14 Hours

Unit II

Unsupervised Learning Networks and Introduction to Classical Sets and Fuzzy Sets
Introduction, Fixed Weight Competitive Nets, Maxnet, Hamming Network, Kohonen Self-Organizing Feature Maps, Learning Vector Quantization, Counter Propagation Networks, Adaptive Resonance Theory Networks. Special Networks - Introduction to various networks.
Crisp Sets and Fuzzy Sets - operations. Classical Relations and Fuzzy Relations - Cardinality, Properties and composition. Tolerance and equivalence relations. Membership functions- Features, Fuzzification. *membership value assignments, Defuzzification*

15 Hours

Unit III

Fuzzy Logic and Genetic Algorithm Classical& Fuzzy logic, Operations, Boolean Logic, Multivalued Logics, Fuzzy Rule Base and Approximate Reasoning ,Fuzzy Decision making ,Fuzzy Logic Control Systems.
Introduction to GA, Traditional Optimization and search techniques, Search space, Operators: Encoding, Selection, Crossover and Mutation. Stopping Condition of GA.
Fuzzy arithmetic and Fuzzy measures

15 Hours

Unit IV

Support Vector Machine and Applications of Soft Computing Introduction, optimal hyper plane for linearly separable pattern, linear classifier, nonlinear classifier problem, optimal plane for non-separable pattern, example XOR problem, and support vector machine for non-linear regression, summary and discussion. A fusion Approach of Multispectral Images with SAR Image for flood area analysis, Optimization of TSP using GA Approach and GA-Fuzzy system for Control of flexible Robots.
Hybrid soft computing techniques

16 Hours

Total: 60 Hours

Text Book (s):

1. S N Sivanandam, S N Deepa, Principles of Soft Computing, Wiley India, 2011
2. V. Kecman, Learning and Soft computing, Pearson Education, India

Reference Book (s):

1. Fakhreddine O Karray, Clarence D Silva, Soft Computing and Intelligent System Design, Pearson Edition, 2004.
2. Guanrong Chen, Trung Tat Pham, Chapman & Hall/CRC, Introduction to Fuzzy Systems, 2009.
3. S. Haykins, Neural networks: a comprehensive foundation, Pearson Education, India

Sample Question (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	25	15	--
Understand	50	35	--
Apply	25	50	--
Analyse			50
Evaluate	--	--	50
Create	--	--	--
Total (%)	100	100	100

Understand

1. Explain about soft computing?
2. Classify supervised learning and unsupervised learning?
3. Summaise the difference between conventional control system and Fuzzy control

Apply

1. Demonstratre the application of Fuzzy logic in Indusrtial manfacturing?
2. Show the differences between Traditional Algorithms and Genetic Algorithm
3. A genetic algorithm is to be used to evolve a binary string of length n containing only 1s. The initial population is a randomly generated set of binary strings of length n. Give a suitable fitness function for this problem.

Analyze

1. If the population size in a genetic algorithm is restricted to 1, what search algorithm does it correspond to? Justify your answer.
2. Consider two fuzzy sets X and Y with the following membership functions: X = {(x1/0.4, (x2/0.7), (x3/0.8), (x4/1)} Y = {(x1/0.3), (x2/0.6), (x3/0.5), (x4/).9)} Resolve: XυY, X∩Y, X-Y, X+Y, X*Y
3. Consider A NN interconnected system which consists of a set of NN models. Establish a linear difference inclusion state (LDI) space representation for the dynamics. By Lyaponov's direct method derive the stability criteria for guaranteeing the asymptotic stability of NN interconnected systems.

[Open Book Examination Question]

Evaluate

1. Suppose a genetic algorithm uses chromosomes of the form x = abcdefgh with a fixed length of eight genes. Each gene can be any digit between 0 and 9. Let the fitness of individual x be

calculated as: f(x) = (a + b) − (c + d) + (e + f) − (g + h) and let the initial population consist of four individuals with the following chromosomes: x1 = 6 5 4 1 3 5 3 2 x2 = 8 7 1 2 6 6 0 1 x3 = 2 3 9 2 1 2 8 5 x4 = 4 1 8 5 2 0 9 4. Evaluate the fitness of each individual, showing all your workings, and arrange them in order with the fittest first and the least fit last.

2. Suggest a suitable evolutionary computing technique for finding optimized Economic Load Dispatch. Support your answer by providing detailed analysis
3. Consider four travel packages offered by Thomas Cook, Club Mahindra, World around, and Himalaya Travels. We want to choose one. Their costs are INR 100,000, INR 200,000 , INR 150,000 and INR 175,000. Their trave time in hours are 1 l 50, 200, 100,and 125 respectively. They are viewed as interesting with degrees 0.4 , 0.3 ,0.6 ,0.5. Define your own fuzzy set of acceptable travel times. Then determine the fuzzy set of interesting travel packages. whose cost and travel times are acceptable and use this set to choose one of your own packages

   [Open Book Examination Question]

21ECH42 Audio Signal Processing

4 0 0 4

Course Outcomes

1. Explain the audio quality measures
2. Demonstrate the masking in the time and frequency domain
3. Classify the audio coding techniques
4. Demonstrate the process of digital audio restoration
5. Outline the time scale and pitch scale modification of audio signals
6. Compare time domain and frequency domain techniques

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PSO_2
1	2	-	-	2
2	2	-	-	2
3	3	2	2	3
4	3	2	2	3
5	2	-	-	2
6	2	-	-	2

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Audio quality determination based on perceptual measurement techniques

Introduction, Basic measuring philosophy, Subjective versus objective perceptual testing, The perceptual audio quality measure (PAQM), Validation of the PAQM on speech and music codec databases

Cognitive effects in judging audio quality, ITU Standardization.

14 Hours

Unit II

Perceptual Coding of High-Quality Digital Audio

Psychoacoustics: Masking in the Frequency Domain, Masking in the Time Domain, Variability between listeners, Basic ideas of perceptual coding: Basic block diagram, Additional coding tools, Perceptual Entropy, Description of coding tools: Filter banks, Perceptual models, Quantization and coding, Joint stereo coding, Prediction, Multi-channel: to matrix or not to matrix, Applying the basic techniques: real coding systems, , MPEG-2 Advanced Audio Coding (MPEG-2 ACC)

MPEG Audio , MPEG-4 Audio.

16 Hours

Unit III

Digital Audio Restoration

Modeling of audio signals, Click removal: Modeling of clicks, Detection, Replacement of corrupted samples, Statistical methods for the treatment of clicks, Correlated noise pulse removal, Background noise reduction by short-time spectral attenuation.

Pitch variation defects

14 Hours

Unit IV

Time and Pitch scale modification of audio signals

Notations and definitions: An underlying sinusoidal model for signals, A definition of time-scale and pitch-scale modification, Frequency-domain techniques: Methods based on the short-time Fourier transform, Methods based on a signal model, Time-domain techniques: Principle, Pitch independent methods, Periodicity-driven methods, Formant modification: Time-domain techniques, Frequency-domain techniques, Generic problems associated with time or pitch scaling.

Time-domain vs frequency-domain techniques

16 Hours

Total: 60 Hours

Text Book (s):

1. Mark Kahrs, Karlheinz Brandenburg, “Applications of DSP to Audio and Acoustics”, Kluwer Academic Publishers.
2. Yiteng (Arden) Huang, Jacob Benesty, “2. Audio signal processing for nextgeneration multimedia communication systems”, Kluwer Academic Publishers 2004.

Reference Book (s):

1. Udo Zölzer, “Digital Audio Signal Processing”, Wiley publishers.
2. Andreas Spanias, Ted Painter and Venkatraman, “Audio signal processing and coding”, Wiley publishers.

Sample Question (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam[1] (%)
Remember	--	--	--
Understand	70	25	--
Apply	30	75	50
Analyse	--	--	50
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Understand

1. How can Validate the PAQM on speech and music codec databases?
2. Explain ITU standardization.
3. Illustrate basic block diagram of perceptual coding.
4. Interpret the process of click removal.
5. Explain the methods based on short time Fourier transform.

Apply

1. Access the importance of subjective and objective measures of audio quality.
2. Demonstrate the cognitive effects that are important in subjective audio quality
3. Outline the basic tools of MPEG-2 AAC system.
4. Demonstrate the ways of using the phase-vocoder for pitch scaling operations.

[Open Book Examination Question]

Analyse

1. Compare and contrast time domain and frequency domain techniques.
2. Organize different filter banks which are used for audio coding purposes.
3. Outline the main features of intensity stereo coding.
4. Outline the process of background noise reduction by short-time spectral attenuation
5. Discuss the generic problems associated with time or pitch scaling

[Open Book Examination Question]

21ECH43 Statistical Signal Processing

4 0 0 4

Course Outcomes

1. Explain about random variables.
2. Classify the random processes, wide-sense stationary processes.
3. Demonstrate Estimation Theory.
4. Outline the signal in presence of white Gaussian Noise.
5. Summarize the characteristics of kalman Filtering.
6. Illustrate the applications of filtering.

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PSO_1
1	2	-	-	2
2	2	-	-	3
3	3	2	2	3
4	3	2	2	3
5	2	-	-	2
6	2	-	-	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Review of random variables

Distribution and density functions, moments, independent, uncorrelated and orthogonal random variables, Central Limit theorem, Random processes, wide-sense stationary processes, autocorrelation and auto covariance functions.

Gaussian Process and White noise process

14 Hours

Unit II

Parameter Estimation Theory

Bayesian estimation, Principle of estimation and applications, Properties of estimates, unbiased and consistent estimators, the methods of maximum likelihood and its properties.

Efficient estimators; Criteria of estimation

16 Hours

Unit III

Estimation of signal in presence of white Gaussian Noise and Spectral analysis

Linear Minimum Mean-Square Error Filtering: Wiener Hoff Equation, FIR Wiener filter, Causal IIR Wiener filter.

Estimated autocorrelation function, periodogram, Averaging the periodogram (Bartlett Method), Welch modification.

Introduction to parametric and frequency methods

16 Hours

Unit IV

Kalman filtering

State-space model and the optimal state estimation problem, discrete Kalman filter, extended Kalman filter using Matlab.

14 Hours

Total: 60 Hours

Text Book (s):

1. Discrete Random Signals and Statistical Signal Processing, By Charles W. Therrien,Prentice Hall Signal Processing Series.
2. M. Hays: Statistical Digital Signal Processing and Modelling, John Willey and Sons, 1996.
3. M.D. Srinath, P.K. Rajasekaran and R. Viswanathan: Statistical Signal Processing with Applications, PHI, 1996

Reference Book (s):

1. Steren M.Kay , Fundamentals of Statistical signal processing : Estimation theory upper saddle river , New Jersy , USA : Prentics Hall , 1993

2. M. H. Hayes, Statistical Digital Signal Processing and Modeling, John Wiley & Sons, Inc.,
3. D.G. Manolakis, V.K. Ingle and S.M. Kogon: Statistical and Adaptive Signal Processing,McGraw Hill, 2000.
4. Monson H. Hayes, 'Statistical Digital Signal Processing and Modeling", John Wiley and Sons, Inc, Singapore, 2002

Sample Question (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember			--
Understand	70	25	--
Apply	30	75	50
Analyse	--		50
Evaluate	--	--	
Create	--	--	--
Total (%)	100	100	100

Understand

1. State the Distribution and density functions.
2. Recall Bayesian estimation
3. Define Wiener Hoff Equation
4. Recall State-space model

Apply

1. Demonstrate uncorrelated and orthogonal random variables
2. Assess wide-sense stationary processes
3. Design FIR Wiener filter
4. Design discrete Kalman filter transfer function
   [Open Book Examination Question]

Analyse

1. Discuss Central Limit theorem.
2. Explain the methods of maximum likelihood and its properties.
3. Determine the estimated autocorrelation function, periodogram
4. How to solve optimal state estimation problem
   [Open Book Examination Question]

21ECH44Computer Vision

4 0 0 4

Course Outcomes

1. Interpert fundamental image processing techniques required for computer vision
2. Assess shape analysis, chain codes and other region descriptors
3. Assess Hough Transform for line, circle, and ellipse detections
4. Predict 3D vision techniques
5. Outline motion related techniques
6. Exemplify the applications using computer vision techniques

COs – POs Mapping

COs	PO_1	PO_2	PSO_2
1	2	-	2
2	3	2	3
3	3	2	3
4	3	2	3
5	3	2	3
6	2	-	2

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Image Processing Foundations and shape analysis

Review of image processing techniques, classical filtering operations, thresholding techniques, edge detection techniques, corner and interest point detection, mathematical morphology - texture. Binary shape analysis: connectedness , object labeling and counting, size filtering, distance functions, skeletons and thinning, deformable shape analysis, boundary tracking procedures, active contours, shape models and shape recognition, boundary length measures, boundary descriptors, chain codes, Fourier descriptors, region descriptors, moments.

centroidal profiles, handling occlusion

16 Hours

Unit II

Hough Transform

Hough Transform for line detection, foot-of-normal method, line localization, line fitting, RANSAC for straight line detection, HT based circular object detection, accurate center location, speed problem, ellipse detection, Case study: Human Iris location, hole detection, generalized Hough Transform (GHT), spatial matched filtering, GHT for ellipse detection, object location

GHT for feature collation

14 Hours

Unit III

3D Vision and Motion

Methods for 3D vision, projection schemes, shape from shading, photometric stereo, shape from texture, shape from focus, active range finding, surface representations, point-based representation, volumetric representations, 3D object recognition, 3D reconstruction. Introduction to motion: triangulation, bundle adjustment, translational alignment, parametric motion, spline-based motion, layered motion.

*Optica*lflow,

16 Hours

Unit IV

Applications

Application: Photo album, Face detection, Face recognition, Eigen faces, Active appearance, 3D shape models of faces Application: Surveillance – foreground, background separation, particle filters, Chamfer matching, tracking, occlusion – combining views from multiple cameras. Human gait analysis Application: In-vehicle vision system- locating roadway, road markings.

identifying road signs, locating pedestrians

14 Hours

Total: 60 Hours

Text Book (s):

1. D. L. Baggio, "Mastering OpenCV with Practical Computer Vision Project", Packet Publishing, 2012.
2. E. R. Davies, "Computer & Machine Visio", Fourth Edition, Academic Press, 2012.

Reference Book (s):

1. Jan Erik Solem, "Programming Computer Vision with Python: Tools and algorithms for analyzing images", O'Reilly Media, 2012.
2. Mark Nixon and Alberto S. Aquado, "Feature Extraction & Image Processing for Computer Visio", Third Edition, Academic Press, 2012.
3. R. Szeliski, "Computer Vision: Algorithms and Applications", Springer 2011.
4. Simon J. D. Prince, "Computer Vision: Models, Learning, and Inferenc", Cambridge University Press, 2012.

Sample Question (S)

Internal Assessment Pattern

Cognitive Level	Int. Test 1 (%)	Int. Test 2 (%)	Open Book Exam (%)
Remember	--	--	--
Understand	70	25	--
Apply	30	75	50
Analyse	--	--	50
Evaluate	--	--	--
Create	--	--	--
Total (%)	100	100	100

Understand

1. How do you address the issue of the edge pixels being used less than the central pixels during convolutional operation?
2. Infer the languages supported by Computer vision
3. Represent he formula For calculating D4 And D8 Distance
4. Explain Volumetric representations of 3D Vision.
5. Exemplify the applications of computer vision

Apply

1. Assess the procedures for active contours based on boundary tracking
2. Demonstrate the concepts based on distance functionin binary shape analysis
3. Demonstrate Hough Transform based circular object detection with an example
4. Assess the various Projection schemes for 3D vision and motion
5. Implement the 3D shape models of face recognition with an example

[Open Book Examination Question]

Analyse

1. Compare and contrast various filtering and thresholding techniques.
2. Organize different approaches for body shape analysis.
3. Outline the Generalized Hough Transform for ellipse detection and object location.
4. Differentiate spline based motion and layered motion in 3D computer vision
5. Outline the impact of human gait analysis for loacating pedestrians in traffic signals.

[Open Book Examination Question]